Doc. Version:	0.6
Total Pages:	56
Date :	2007.1.18

Product Specification

1.7″ COLOR TFT-LCD MODULE

MODEL NAME: A017CN01 V4

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	25/May/2006		New create
0.1	16/May/2006		Update EE part.
0.2	03/July/2006	6,32~33	Update EE part
0.3	22/Sep/2006	25 ~ 27	Add internal AVDD applicatoin circuit
		29 ~ 56	Remove the related data about 1 LED.
		29	Add register function a. Gamma select b. Internal voltage select c. Internal voltage enable select
0.4	04/Oct/2006	21~27	Add a mark for「switch」
0.5	05/Oct/2006	8	Modify suggested LED current
0.6	18/Jan/2007	40,43	reminder for mchanical designer

Content

A. Physical specifications

No.	Item	Specification	Remark
1	Display resolution (dot)	480 (W) × 240 (H)	
2	Active area (mm)	34.08 (W) × 25.56 (H)	
3	Screen size (inch)	1.68 (Diagonal)	
4	Dot pitch (mm)	0.071 (W) × 0.1065 (H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension (mm)	41.58 (W) × 37.26(H) × 2.8 (D)	Note 1
7	Weight (g)	9	
8	Panel surface treatment	Hard coating (3H)	

Note 1: Refer to Fig. 4

B. Electrical specifications

1. Pin assignment

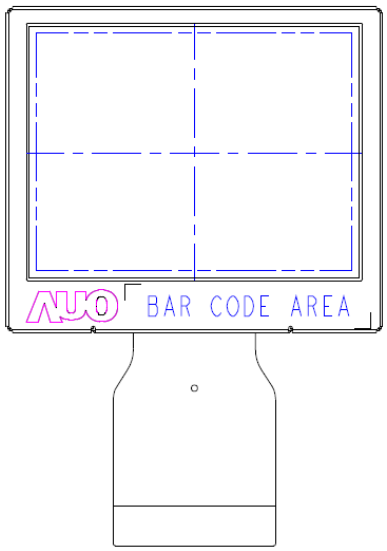
Pin no	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode driving voltage	
2	VGLC	C	Pins to connect capacitance for negative high power supply	
3	VGL	C	Negative low power supply for gate driver output: -12.5V	
4	C4P	C	Pins to connect capacitance for power circuitry	
5	C4M	C	Pins to connect capacitance for power circuitry	
6	VGH	C	Positive power supply for gate driver output: +12.5V	
7	FRP	O	Frame polarity output for VCOM	
8	VCAC	C	Define the amplitude of the VCOM swing	
9	Vint3	C	Intermediate voltage for charge Pump	
10	C3P	C	Pins to connect capacitance for power circuitry	
11	C3M	C	Pins to connect capacitance for power circuitry	
12	Vint2	C	Intermediate voltage for charge Pump	
13	C2P	C	Pins to connect capacitance for power circuitry	
14	C2M	C	Pins to connect capacitance for power circuitry	
15	Vint1	C	Intermediate voltage for charge Pump	
16	C1P	C	Pins to connect capacitance for power circuitry	
17	C1M	C	Pins to connect capacitance for power circuitry	
18	PGND	P	Charge Pump Power GND	
19	PVDD	P	Charge Pump Power VDD	
20	DRV	O	Gate signal for the power transistor of the boost converter	
21	LED Anode	P	For Led Anode voltage	
22	GND	P	Digital GND	
23	FB	P/I	Led Cathode and main boost regulator feedback input	
24	AVDD	P	Analog power supply	
25	GND	P	Digital GND	
26	VCC	P	Digital power supply	
27	CS	I	Serial communication chip select	
28	SDA	I/O	Serial communication data input/output	
29	SCL	I	Serial communication clock input	
30	HSYNC	I	Horizontal sync input	
31	VSYNC	I	Vertical sync input	
32	DCLK	I	Clock Input:	
33	D7	I	Data Input: MSB	

34	D6	I	Data Input:	
35	D5	I	Data Input:	
36	D4	I	Data Input:	
37	D3	I	Data Input:	
38	D2	I	Data Input:	
39	D1	I	Data Input:	
40	D0	I	Data Input: LSB	

I: Input; O: Output. P: Power. I/O input/output C: Capacitor pin. P/I: power / input

Note: Definition of scanning direction. Refer to figure as below

TOP



2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND = 0	-0.5	7.0	V	Digital Power Supply
	AV_{DD}	AV_{SS} = 0	-0.5	7.0	V	Analog Power Supply
	PV_{DD}	PV_{SS} = 0	-0.5	7.0	V	Charge Pump Power Supply
Input signal voltage	Data	-	-0.3	3.6	V	
Input signal voltage	VCOM		-2.9	5.2	V	VCOM DC Voltage
Operating temperature	Topa	-	0	60	℃	Ambient temperature
Storage temperature	Tstg	-	-25	70	℃	Ambient temperature

3. Electrical characteristics

a. Typical operating conditions (GND = AVss = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage		V_{CC}	2.7	3.3	3.6	V	Digital Power Supply
		PV_{DD}	3.0	3.3	3.6	V	Analog Power Supply
		PV_{DD}	3.0	3.3	3.6	V	Charge Pump Power Supply
Output Signal Voltage	H Level	V_{OH}	Vcc-0.4	-	VCC	V	
	L Level	V_{OL}	GND	-	GND+0.4	V	
Input Signal Voltage	H Level	V_{IH}	$0.7xV_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
VCOM Voltage		V_{CAC}	5.4	5.8	6.4	V	V
		V_{CDC}	0.6	0.8	1.0	V	V
DRV output voltage		V_{DRV}		0	-	V_{CC}	V
Analog stand by current		Ist	-	-	100	uA	DCLK is stopped

Note 1: A build-in power on reset circuit for PV_{DD} and V_{CC} is provided within the integrated LCD driver IC. The LCD module is in power saving mode in default, and stand-by releasing is required after V_{CC} power on through serial control. Pleaser refer to the register STB setting for detail.

b. Current characteristics (GND = AVss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{CC}	I_{VCC} (Pin 27)	V_{CC}=3.3V	--	2	4	mA	F_{DCLK} = 24.54MHz (UPS052) Other registers are default settings
Input Current for AV_{DD}	I_{AVDD} (Pin 25)	AV_{DD}=3.3V	--	2.5	3	mA	
Input Current for PV_{DD}	I_{PVDD} (Pin 19)	PV_{DD}=3.3V	--	8	10	mA	
Output current	H Level	IOH	-	400	-	uA	
	L Level	IOL	-	-400	-	uA	
Analog stand by current	I_{AST}	AV_{DD}=3.3V	-	50	100	uA	STB = 'L' and all function are shutdown
Digital stand by current	I_{DST}	V_{CC}=3.3V	-	--	100	uA	
DRV output current	I_{DRV}	V_{CC} = 3.0V DRV = 0.7V	-	-	100	mA	

c. LED driving conditions

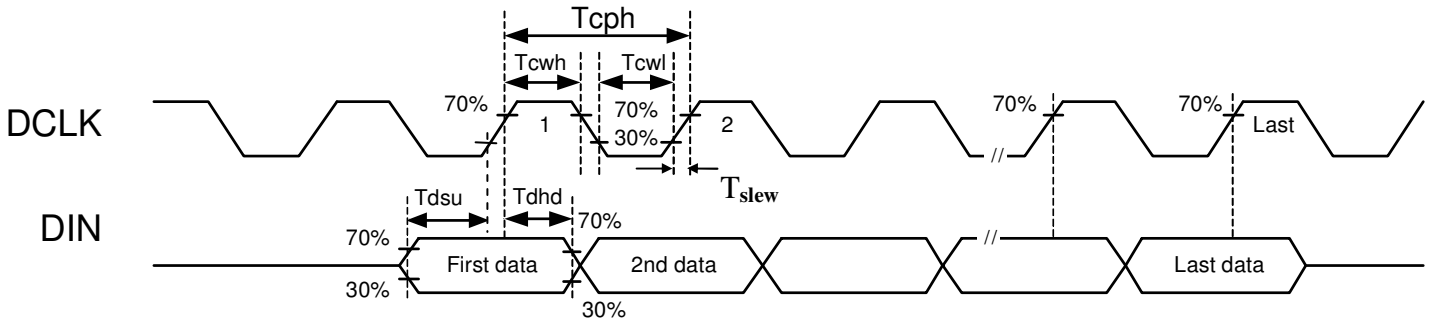
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I_L		25		mA	
LED voltage	V_L	-	3.8	4.4	*V*	Note

Note: LED typical voltage 3.8V is base on internal LED driver (LED driving voltage: Typical =3.2V, Max=3.8V), Please refer to 5. Reference Circuit.

4. AC Timing

a. Digital Signal AC Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.
DCLK cycle time	Tcph (30 – 70%)	9.7MHz (UPS051 mode)	-	103	-	ns
		24.54 MHz (UPS052 320, YUV640 mode)	-	40	-	
		27 MHz (UPS052 320, CCIR656, YUV 720 mode)	-	37	-	
DCLK raising/falling time	Tslew	9.7MHz (UPS051 mode)	-	4.6	-	ns
		24.54 MHz (UPS052 320, YUV640 mode)	-	1.8	-	
		27 MHz (UPS052 320, CCIR656, YUV 720 mode)	-	1.6	-	
DCLK duty cycle	Tcwh/Tcwl		40	50	60	% Tcph
Data set-up time	Tdsu		12	-	-	ns
Data hold time	Tdhd		12	-	-	



b. UPS051 Timing conditions

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	8	9.7	12	MHz	
HSYNC	Period		t_H	580	616	649	DCLK	Note 1
	Display period		t_{hdisp}	480			DCLK	
	Back porch		t_{hbp}	84	100	115	DCLK	
	Front porch		t_{hfp}	0	36	-	DCLK	
	Pulse width		t_{hsw}	1	20	50	DCLK	
VSYNC	Period	Odd	t_V	Note 4	262.5	Note 4	t_H	Note 2, 3, 5, 6
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	11	18	24	t_H	
		Even		10.5	17.5	23.5		
	Front porch	Odd	t_{vfp}	0	4.5	-	t_H	
		Even		0	5	-		
	Pulse width	Odd	t_{vsw}	1	-	-	DCLK	
		Even						
Data set-up time			t_{ds}	12			ns	
Data hold time			t_{dh}	12			ns	

Note 1: UPS051 Horizontal back porch time (t_{hbp}) is adjustable by setting register DDL; requirement of minimum back porch time and minimum front porch time must be satisfied.

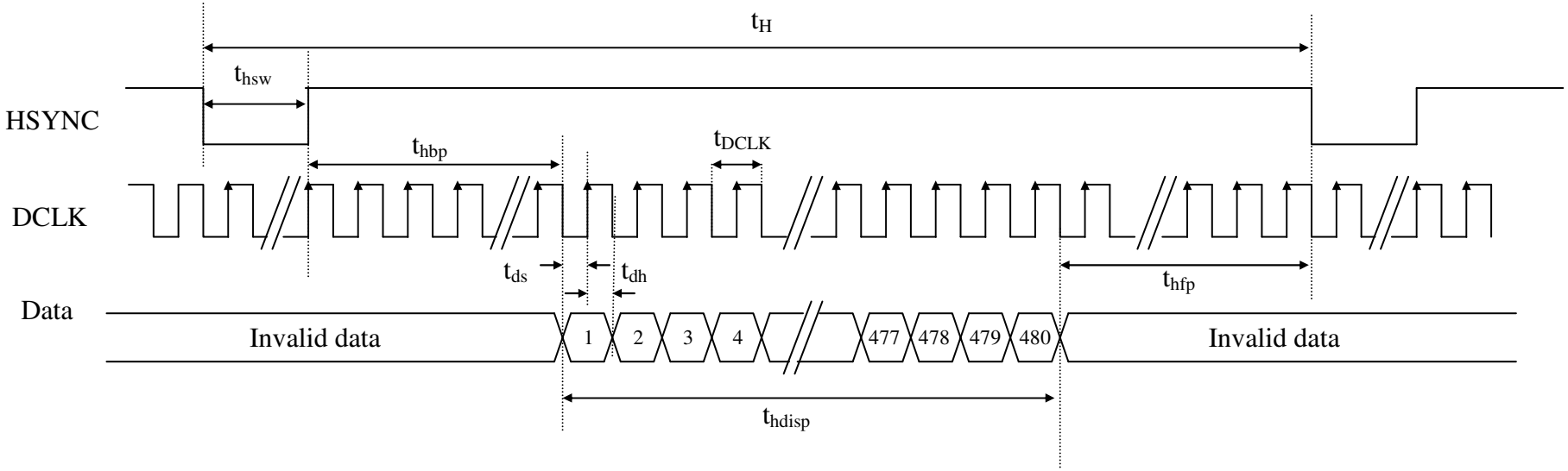
Note 2: UPS051 Vertical back porch time (t_{vbp}) is adjustable by setting register HDL; requirement of minimum back porch time and minimum front porch time must be satisfied.

Note 3: Both interlace and non-interlace mode can be accepted.

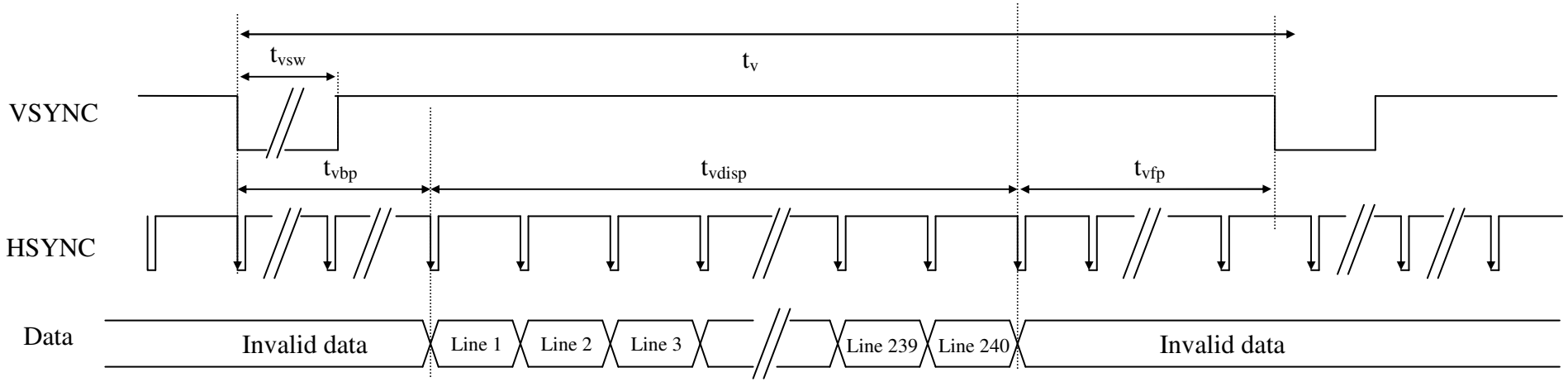
Note 4: Min. and max. value of VSYNC period are related to Hsync period and Vs back porch.

Note 5: This chip supports both interlace & non-interlace mode.

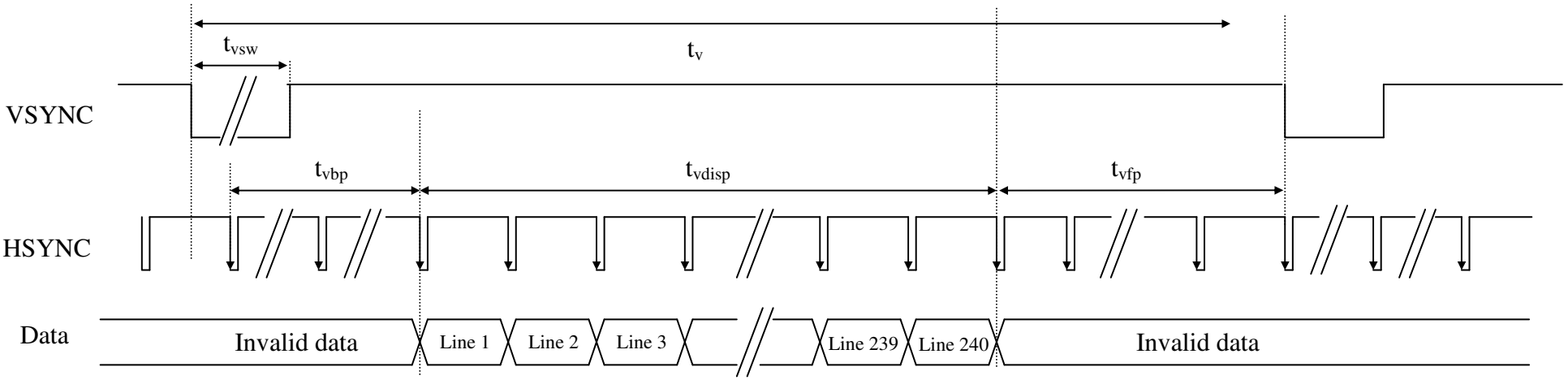
Note 6: Please keep frame over 50 Hz to get the better display quality.



UPS051 Input Horizontal Signal



Odd Field



Even Field

UPS051 Input Vertical Signal

c. UPS052 Timing conditions

c - 1. UPS052 (320 mode 24.545MHz) timing specifications

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	16	24.55	27	MHz	
HSYNC	Period		t_H	1472	1560	1644	DCLK	
	Display period		t_{hdisp}	1280			DCLK	
	Back porch		t_{hbp}	220	252	283	DCLK	
	Front porch		t_{hfp}	0	-	-	DCLK	
	Pulse width		t_{hsw}	1	-	-	DCLK	
VSYNC	Period	Odd	t_V	Note 1	262.5	Note 1	t_H	Note 2, 3
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	11	18	24	t_H	
		Even		10.5	17.5	23.5		
	Front porch	Odd	t_{vfp}	0	4.5	-	t_H	
		Even		0	5	-		
	Pulse width	Odd	t_{vsw}	1	-	-	DCLK	
		Even						

Note 1: Min. and max. value of VSYNC period are related to Hsync period and Vs back porch.

Note 2: This chip supports both interlace & non-interlace mode.

Note 3: Please keep frame over 50 Hz to get the better display quality.

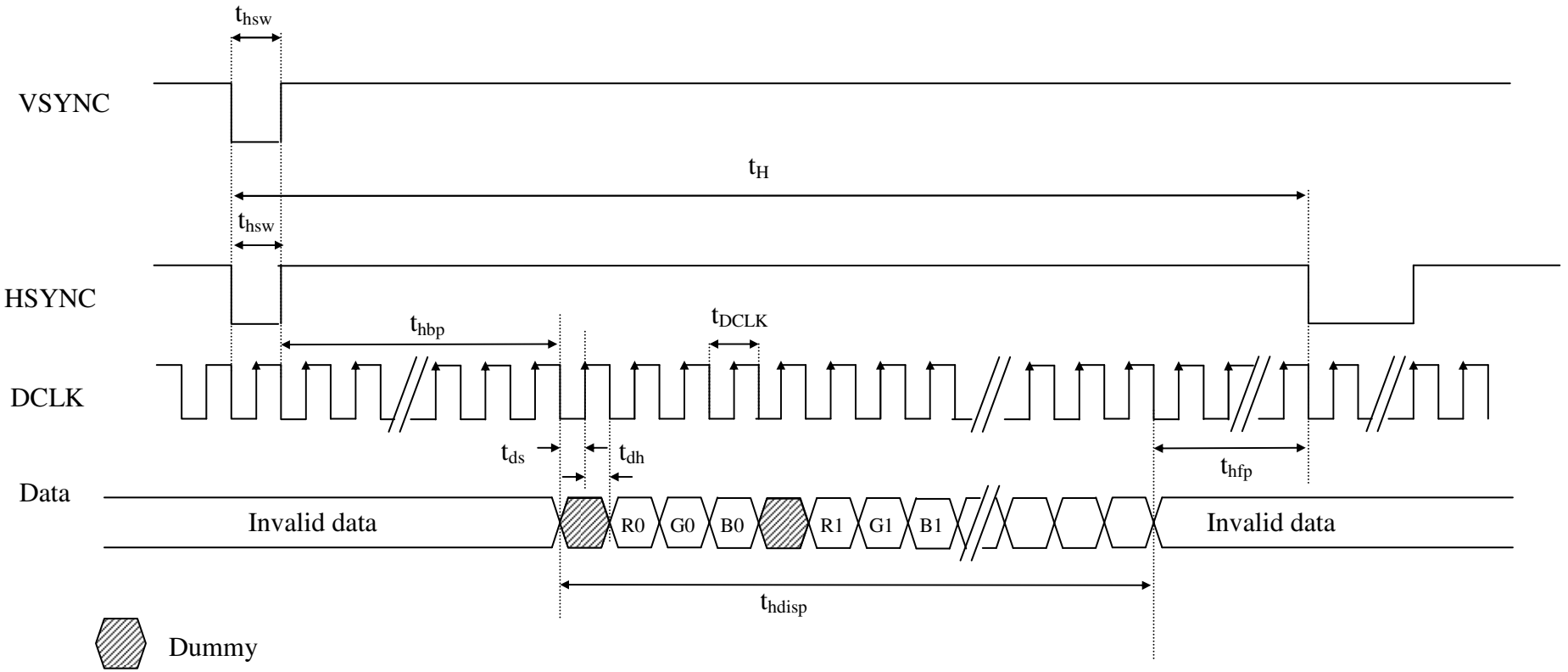
b - 2. UPS052 (360 mode 27MHz) timing specifications

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	16	27	27	MHz	
HSYNC	Period		t_H	1620	1716	1809	DCLK	
	Display period		t_{hdisp}	1440			DCLK	
	Back porch		t_{hbp}	220	252	283	DCLK	
	Front porch		t_{hfp}	0	-	-	DCLK	
	Pulse width		t_{hsw}	1	-	-	DCLK	
VSYNC	Period	Odd	t_V	Note 1	262.5	Note 1	t_H	Note 2, 3
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	11	18	24	t_H	
		Even		10.5	17.5	23.5		
	Front porch	Odd	t_{vfp}	0	4.5	-	t_H	
		Even		0	-	-		
	Pulse width	Odd	t_{vsw}	1	-	-	DCLK	
		Even						

Note 1: Min. and max. value of VSYNC period are related to Hsync period and Vs back porch.

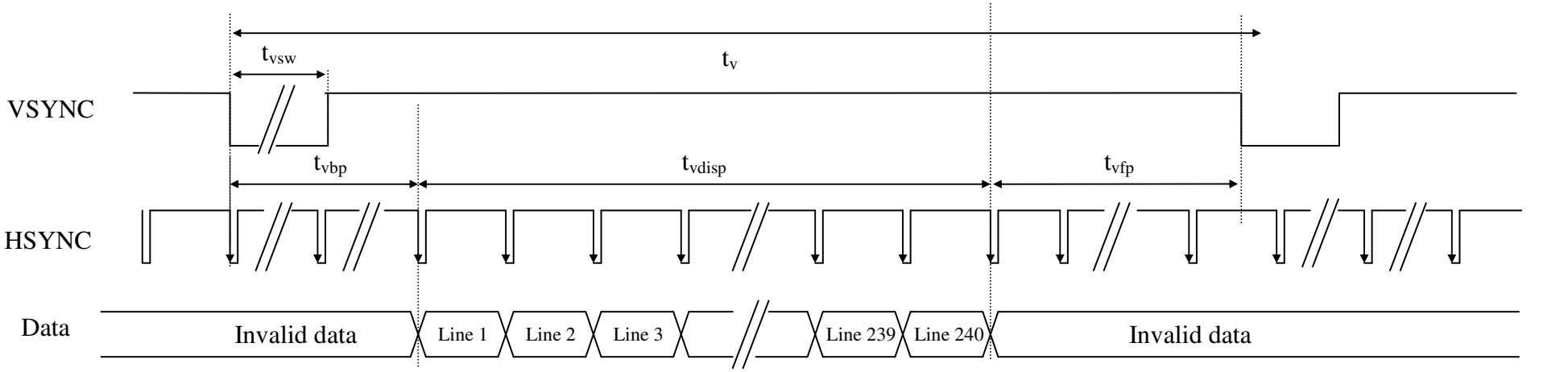
Note 2: This chip supports both interlace & non-interlace mode.

Note 3: Please keep frame over 50 Hz to get the better display quality.

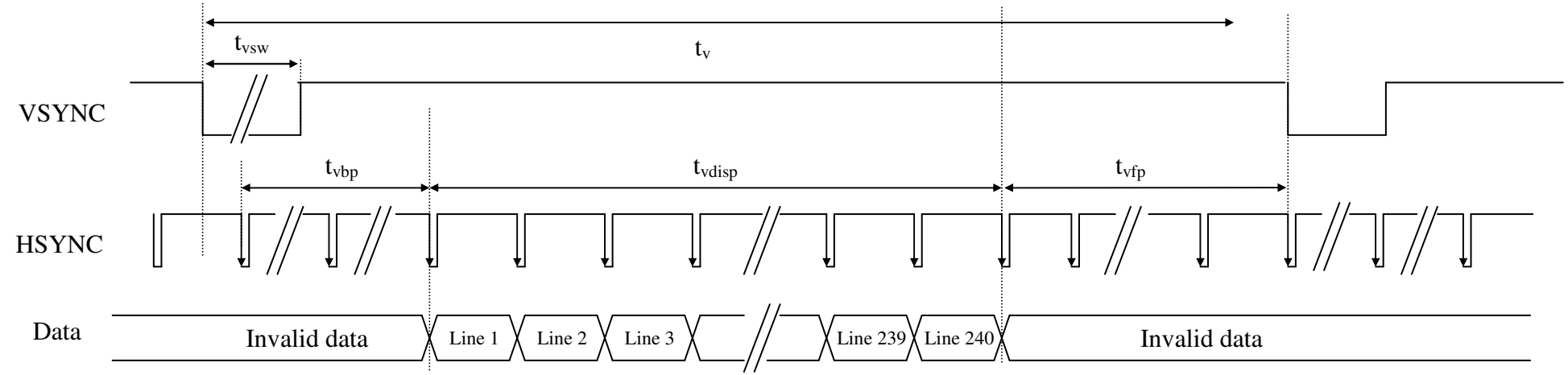


UPS052 Input Horizontal Signal

Note: Please send 00h as blanking data.



Odd Field



Even Field

UPS052 Input Vertical Signal

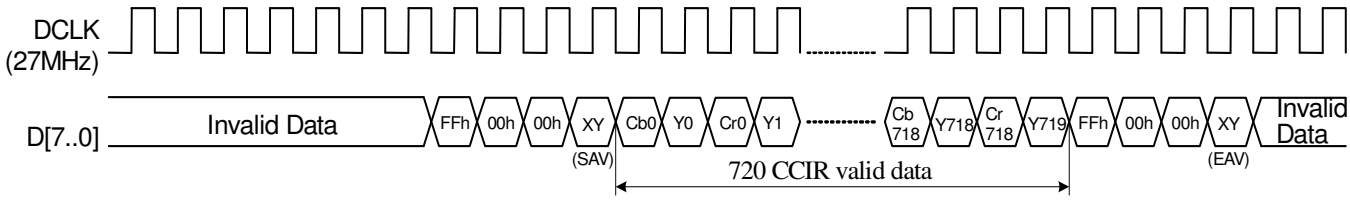
d. CCIR656 Timing conditions

d - 1. CCIR656 timing specifications

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	16	27	27	MHz	
HSYNC	Period		t_H	1620	1716	1809	DCLK	
	Display period		t_{hdisp}	1440			DCLK	
	Back porch		t_{hbp}	241	273	304	DCLK	
	Front porch		t_{hfp}	4	4	4	DCLK	
	Pulse width		t_{hsw}	1	-	-	DCLK	
VSYNC	Period	Odd	t_V	Note 1	262.5	Note 1	t_H	Note 2
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	11	18	24	t_H	
		Even		10.5	17.5	23.5		
	Front porch	Odd	t_{vfp}	0	4.5	-	t_H	
		Even		0	5	-		
	Pulse width	Odd	t_{vsw}	1	-	-	DCLK	
		Even						

Note 1: Min. and max. value of VSYNC period are related to Hsync period and Vs back porch.

Note 2: Please keep frame over 50 Hz to get the better display quality.



CCIR656 Data input format

d- 2. CCIR656 decoding:

FF 00 00 XY signals are involved with HSYNC, VSYNC and Field.

XY encodes following bits:

F = field select

V = indicate vertical blanking

H = 1 if EAV else 0 for SAV

P3-P0 = protection bits

P3 = V⊕H, P2 = F⊕H, P1 = F⊕V, P0 = F⊕V⊕H

⊕ represents the exclusive-OR function.

It is controlled by “End of Video” (EAV) and “Start of Video” (SAV) timing references.

Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	F	V	H	P3	P2	P1	P0

d- 3. CCIR656 to RGB conversion

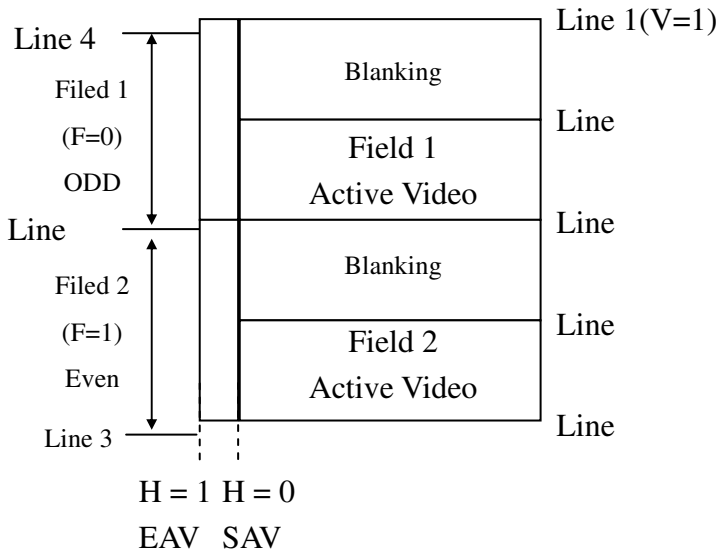
R = 1.164 (Y-16) + 1.596 (Cr-128)

G = 1.164 (Y-16) - 0.813 (Cr-128) - 0.392 (Cb-128)

B = 1.164 (Y-16) + 2.017 (Cb-128)

Where Y: 0~255, Cr: 0~255, Cb: 0~255

d- 4. CCIR656 Vertical Timing Format (NTSC)



Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

e. YUV Timing

e - 1. YUV 640 timing specifications

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	16	24.545	27	MHz	
HSYNC	Period		t_H	1472	1560	1644	DCLK	
	Display period		t_{hdisp}	1280			DCLK	
	Back porch		t_{hbp}	220	252	283	DCLK	
	Front porch		t_{hfp}	0	-	-	DCLK	
	Pulse width		t_{hsw}	1	-	-	DCLK	
VSYNC	Period	Odd	t_V	Note 1	262.5	Note 1	t_H	Note 2
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	11	18	24	t_H	
		Even		10.5	17.5	23.5		
	Front porch	Odd	t_{vfp}	0	4.5	-	t_H	
		Even		0	5	-		
	Pulse width	Odd	t_{vsw}	1	-	-	DCLK	
		Even						

Note 1: Min. and max. value of VSYNC period are related to Hsync period and Vs back porch.

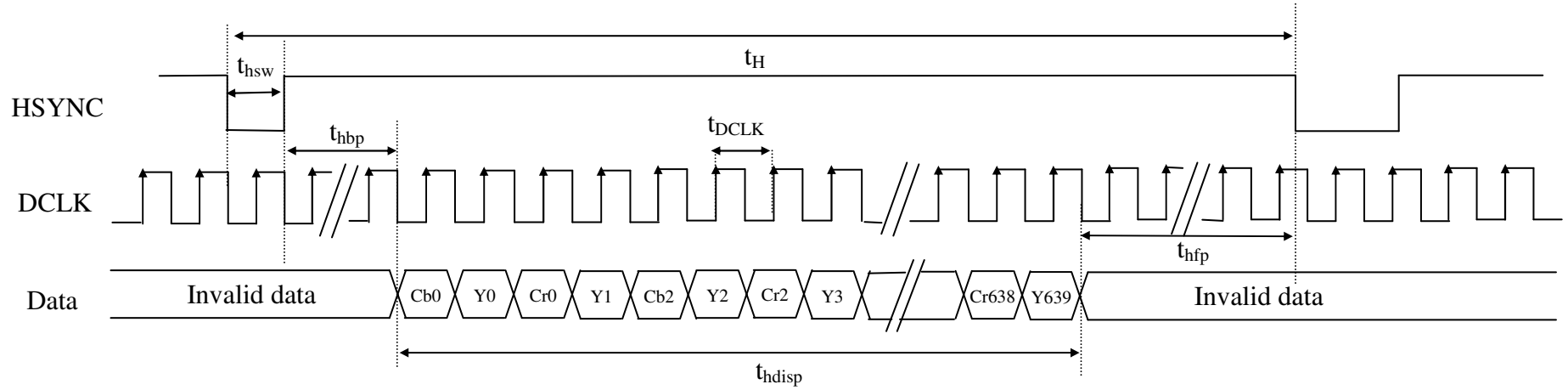
Note 2: Please keep frame over 50 Hz to get the better display quality.

e - 2. YUV 720 timing specifications

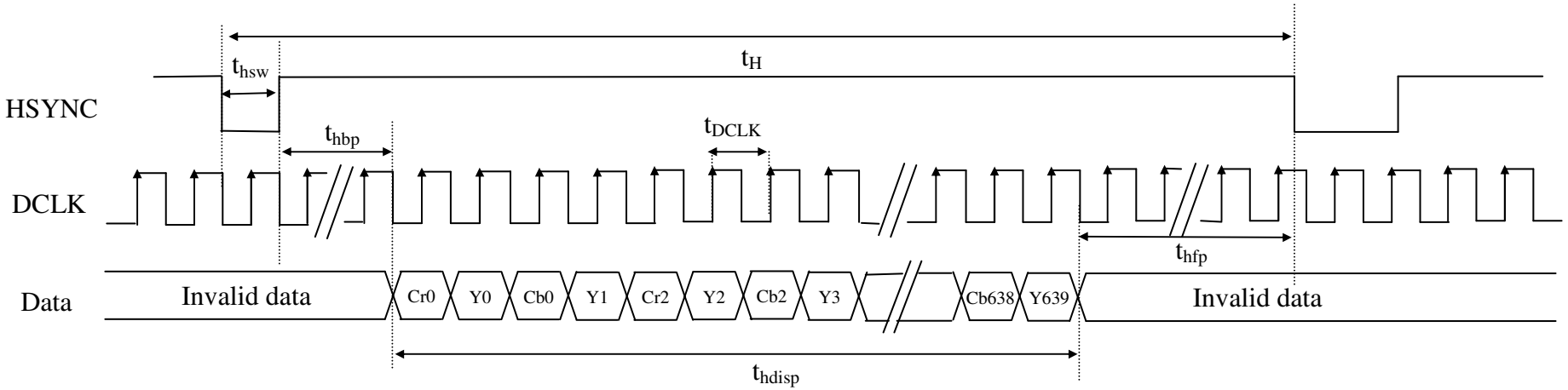
Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	16	27	27	MHz	
HSYNC	Period		t_H	1620	1716	1809	DCLK	
	Display period		t_{hdisp}	1440			DCLK	
	Back porch		t_{hbp}	220	252	283	DCLK	
	Front porch		t_{hfp}	0	24	-	DCLK	
	Pulse width		t_{hsw}	1	20	50	DCLK	
VSYNC	Period	Odd	t_V	Note 1	262.5	Note 1	t_H	Note 2
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	11	18	24	t_H	
		Even		10.5	17.5	23.5		
	Front porch	Odd	t_{vfp}	0	4.5	-	t_H	
		Even		0	5	-		
	Pulse width	Odd	t_{vsw}	1	3	200	DCLK	
		Even						

Note 1: Min. and max. value of VSYNC period are related to Hsync period and Vs back porch.

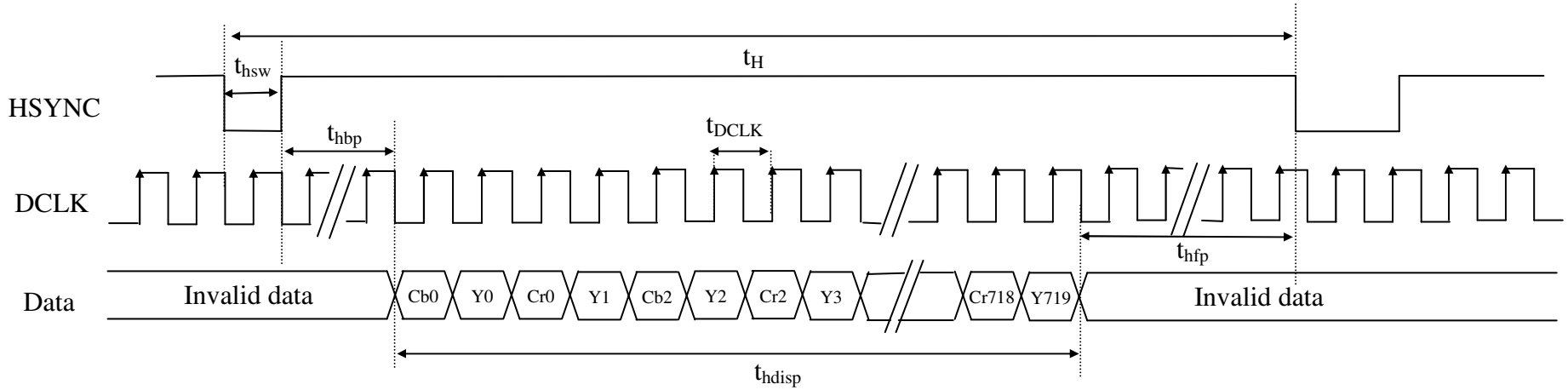
Note 2: Please keep frame over 50 Hz to get the better display quality.



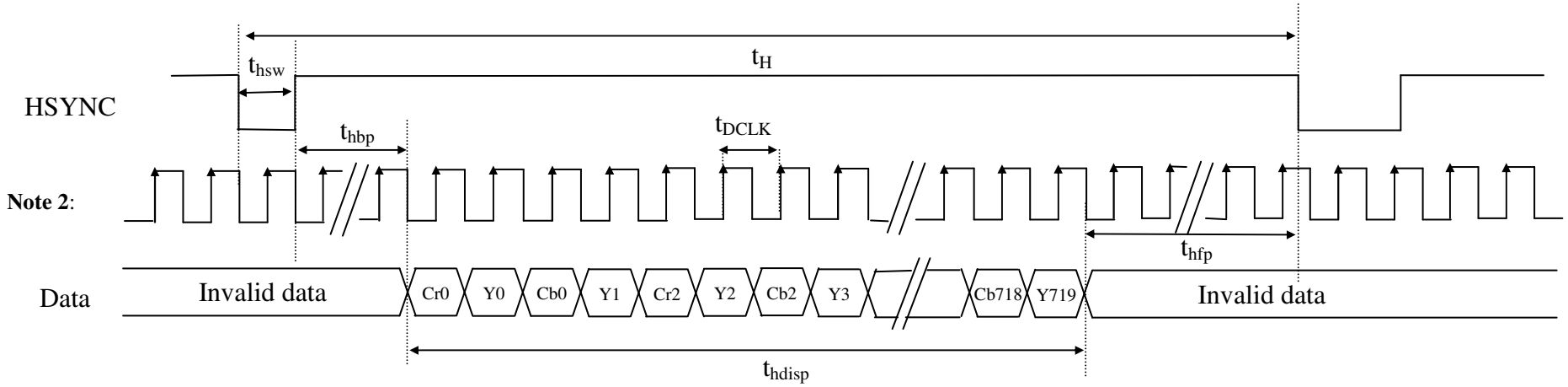
YUV mode A (24.5 MHz) Input Horizontal Signal (SEL = 011)



YUV mode B (24.5 MHz) Input Horizontal Signal (SEL = 101)

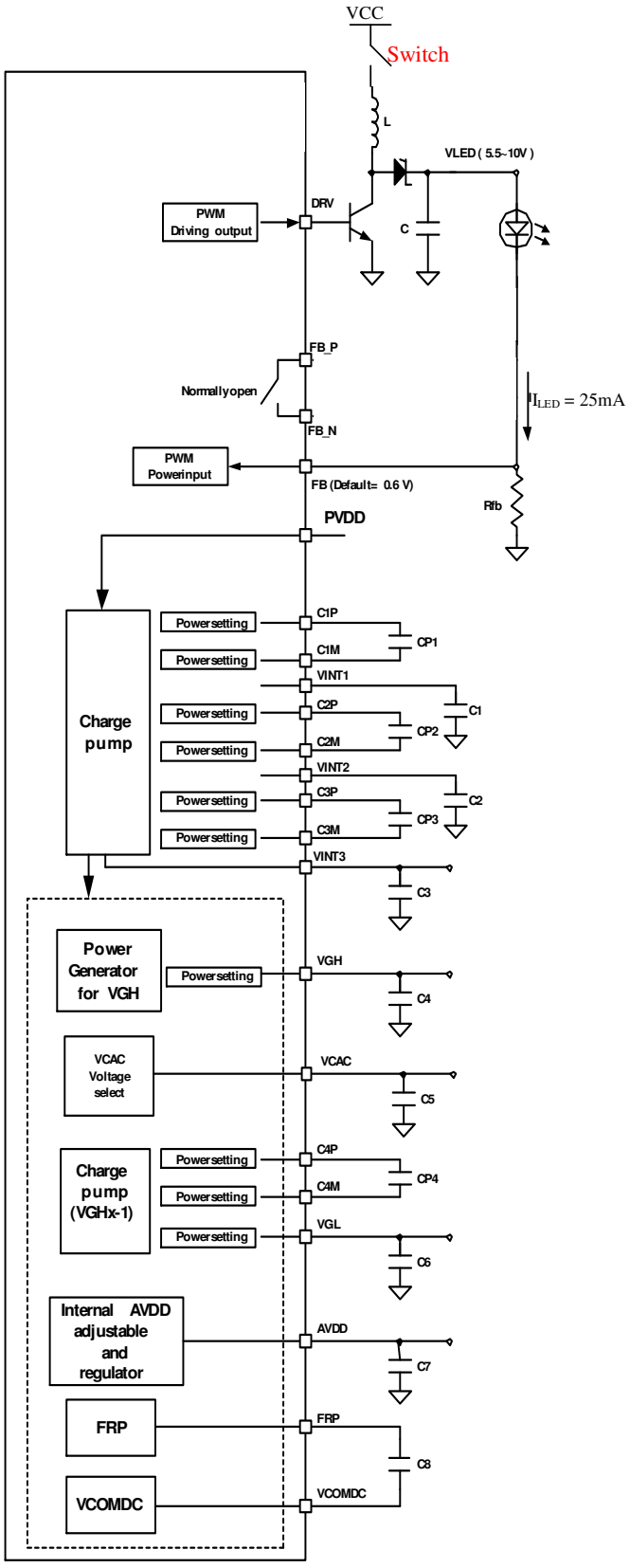


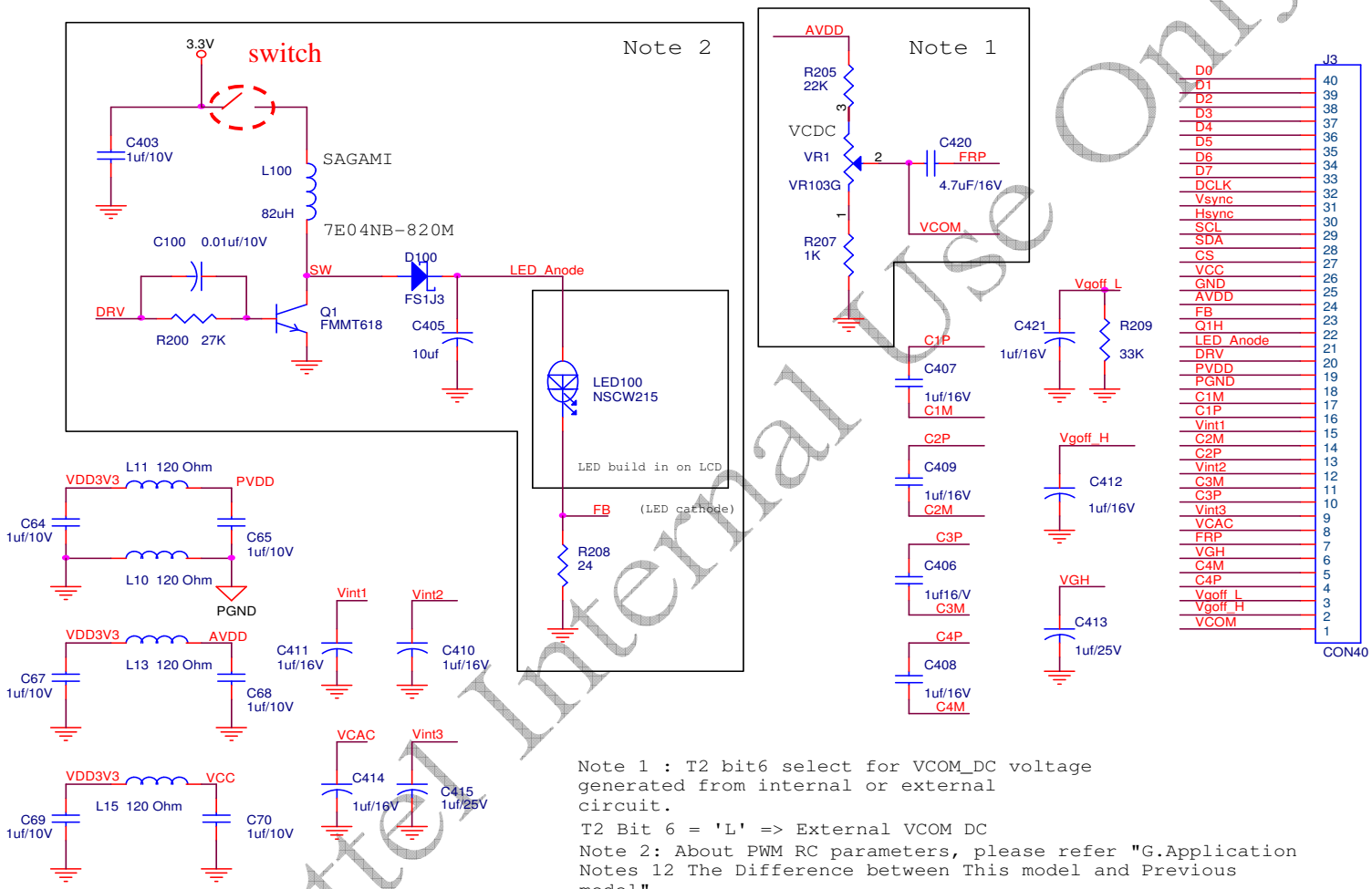
YUV mode A (27 MHz) Input Horizontal Signal (SEL = 100)



YUV mode B (27MHz) Input Horizontal Signal (SEL = 110)

f. Charge Pump Structure

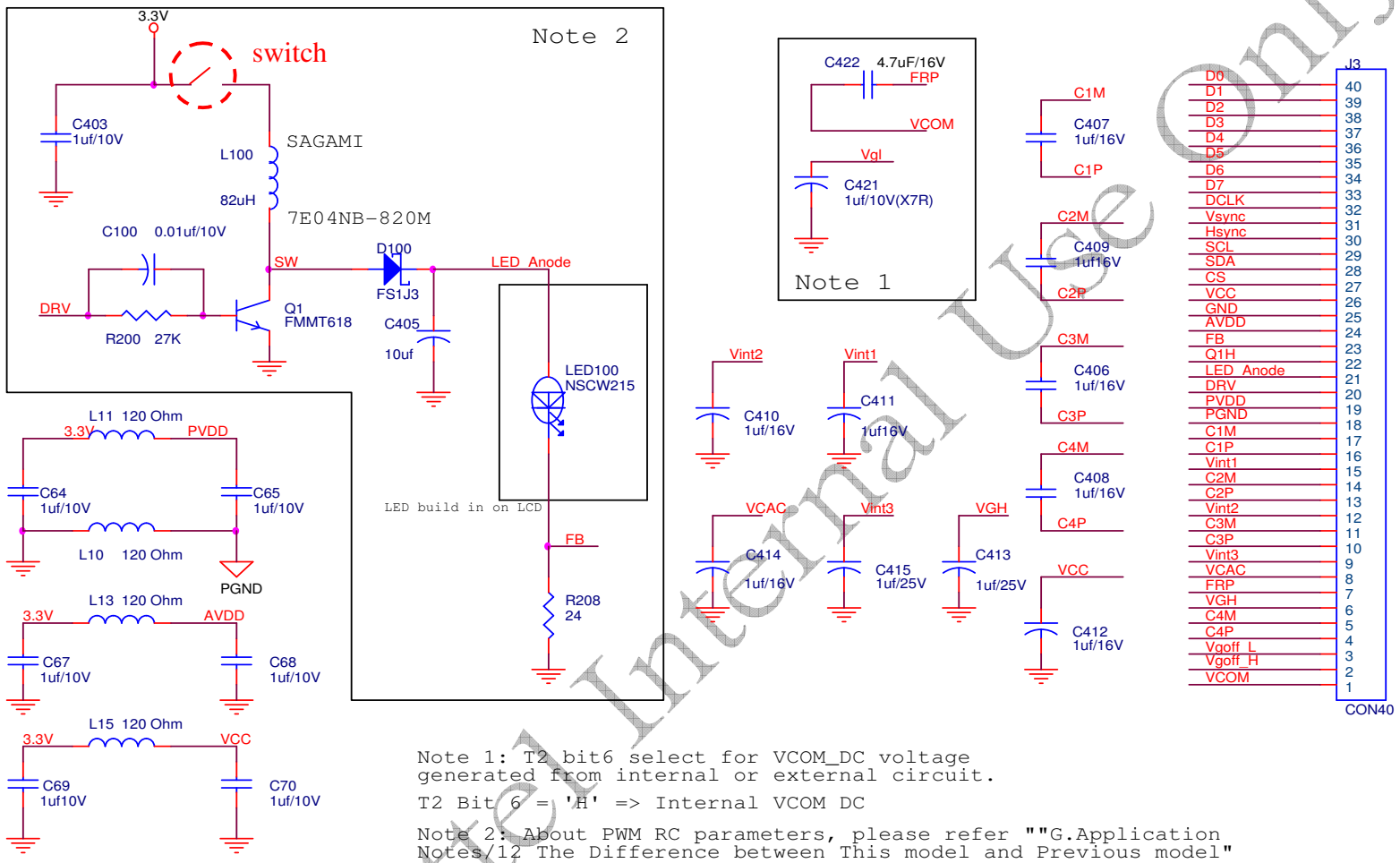




Note 1 : T2 bit6 select for VCOM_DC voltage generated from internal or external circuit.
T2 Bit 6 = 'L' => External VCOM DC
Note 2: About PWM RC parameters, please refer "G.Application Notes 12 The Difference between This model and Previous model"

Note: PWM R/C/L (R200/C100/L100) parameters and component characteristics will effects efficiency and wave like noise. The application circuit is for reference only. If efficiency is not god or wave like noise is serious, please adjust RCL parameters to get best efficiency and display quality

External AVDD +
Internal LED Driver Application Circuit

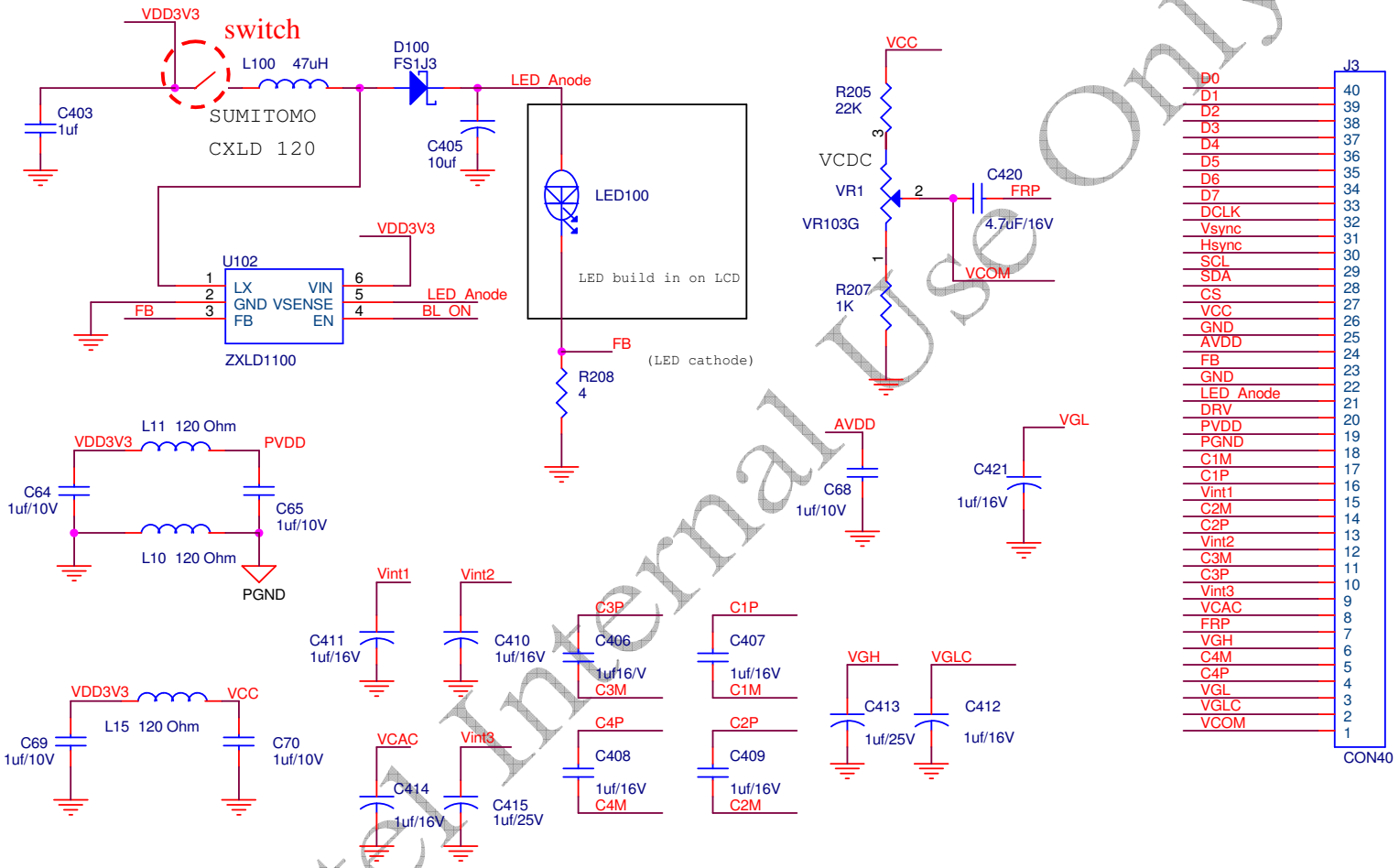


Note 1: T2 bit6 select for VCOM_DC voltage generated from internal or external circuit.
T2 Bit 6 = 'H' => Internal VCOM DC

Note 2: About PWM RC parameters, please refer ""G.Application Notes/12 The Difference between This model and Previous model"

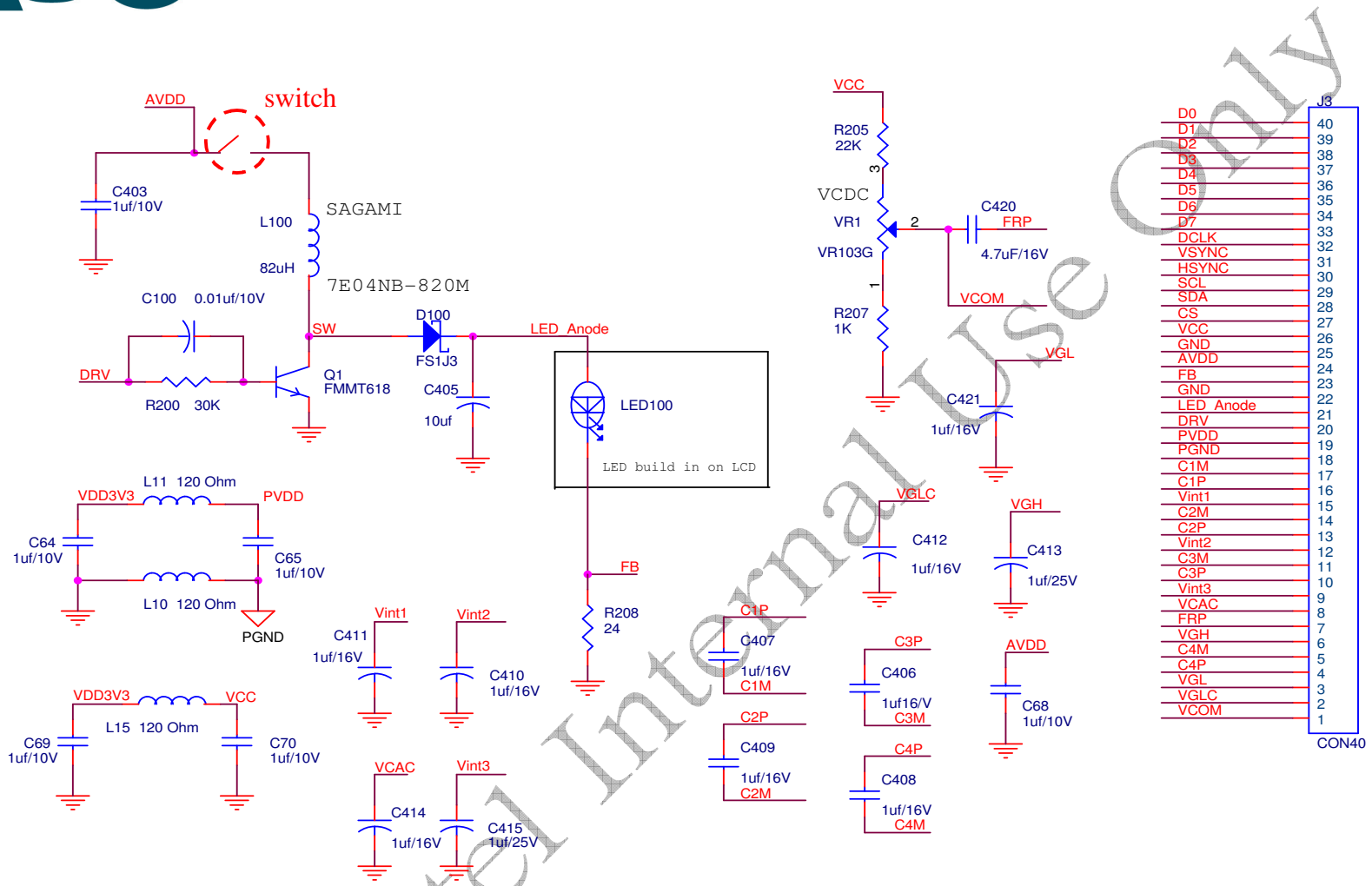
Note: PWM R/C/L (R200/C100/L100) parameters and component characteristics will effects efficiency and wave like noise. The application circuit is for reference only. If efficiency is not god or wave like noise is serious, please adjust RCL parameters to get best efficiency and display quality

External AVDD +
Internal VCOM DC Application Circuit



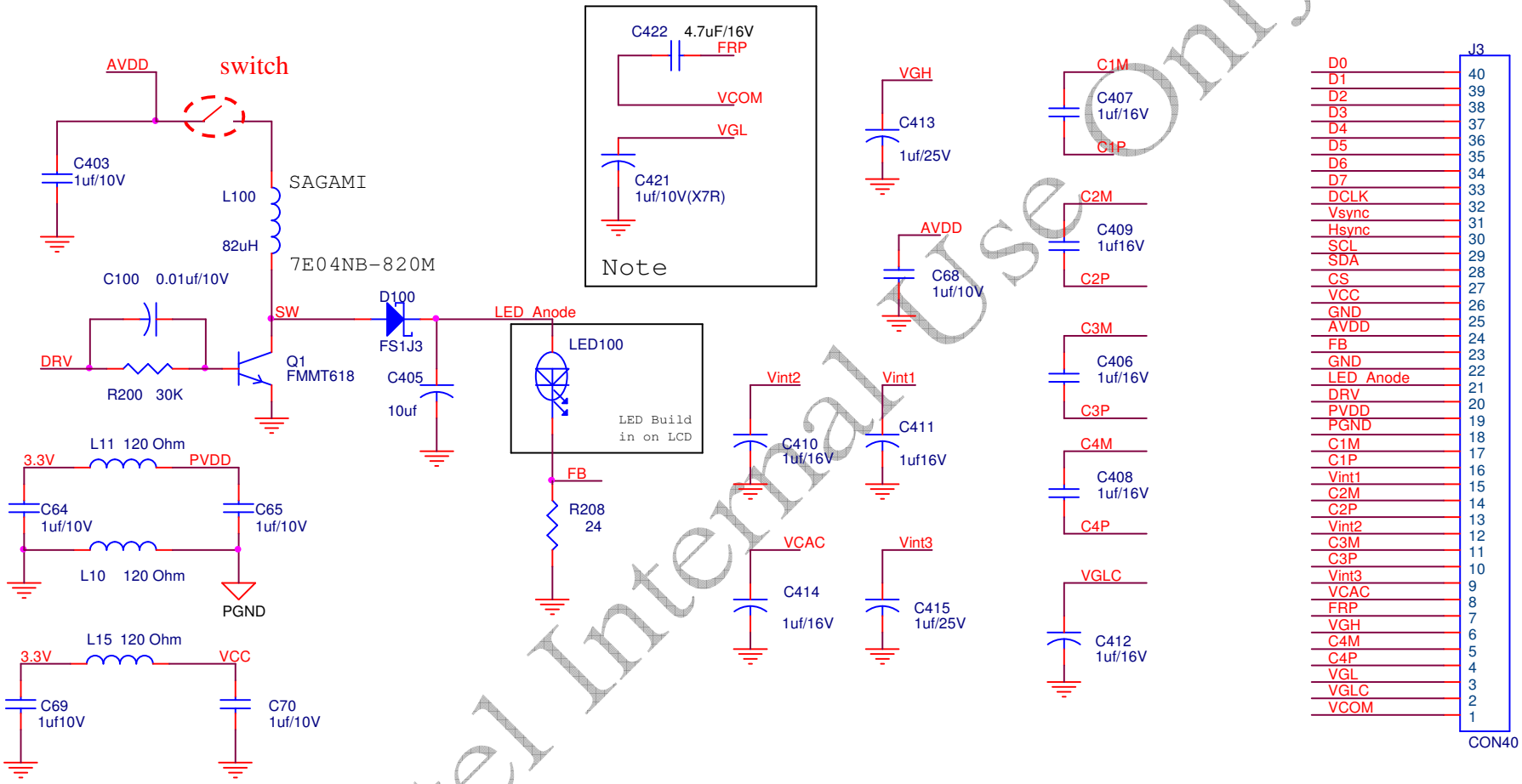
Note 1: ZXLK1100 provide FB voltage 0.1V. If we want to keep LED current at 25mA, R208 have to set to 4 ohm.

Internal AVDD + External LED Driver Application Circuit



Note 1: PWM R/C/L (R200/C100/L100) parameters and component characteristics will effects efficiency and wave like noise. The application circuit is for reference only. If efficiency is not god or wave like noise is serious, please adjust RCL parameters to get best efficiency and display quality

Internal AVDD +
Internal LED Driver Application Circuit

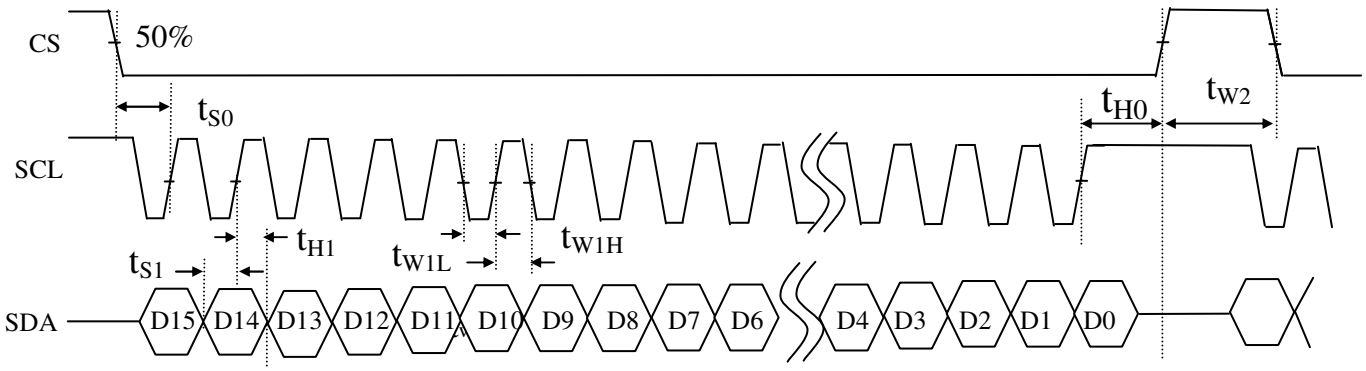


Note 1: PWM R/C/L (R200/C100/L100) parameters and component characteristics will effects efficiency and wave like noise. The application circuit is for reference only. If efficiency is not god or wave like noise is serious, please adjust RCL parameters to get best efficiency and display quality

Internal AVDD +
Internal VCOM DC Application Circuit

6. Serial Interface & Register Table

a. Serial Interface format



Item	Symbol	Conditions	Min	Typical	Max	Unit
Data Setup Time	t_{S0}	SCL to CS	120			ns
	t_{S1}	SCL to SDA	120			ns
Data Hold Time	t_{H0}	SCL to CS	120			ns
	t_{H1}	SCL to SDA	120			ns
Pulse Width	t_{W1L}	SCL pulse width	120			ns
	t_{W1H}	SCL pulse width	120			ns
	t_{W2}	CS pulse width	1000			ns

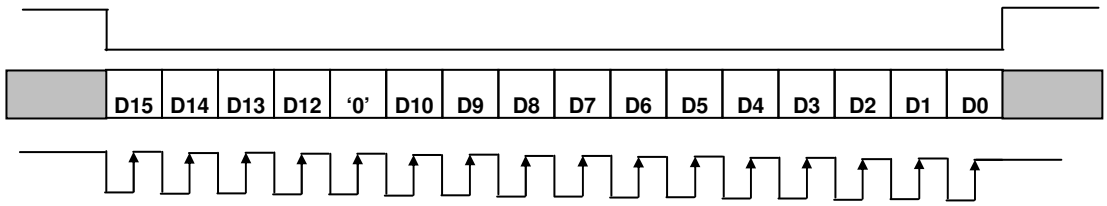
b. Configuration of serial data at SDA terminal is at below

MSB LSB

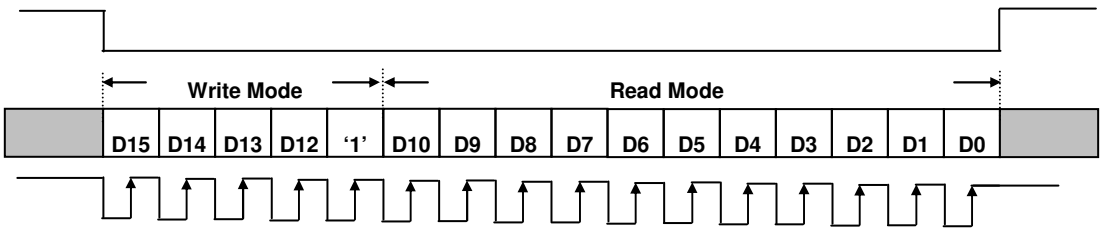
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register address				R/W	DATA										

Note: R/W = '0' ➔ Write mode R/W = '1' ➔ Read mode

b1 – Write Mode waveform



b2 – Read Mode waveform



c. Register parameters

No	ADDRESS				R/W		CONTENT							
	D15	D14	D13	D12	D11	D[10 : 8]	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	W	x	x	x	x	x	GRB	STB	SHDB	SHCB
R1	0	0	1	0	W	x	x	x	Reserved			Reserved	PFON	Reserved
R2	0	1	0	0	W	x	x	x	x	x	FPOL	VSET	U/D	SHL
R3	0	1	1	0	W	x	x	x	x	PALM	PAL	SEL		
R4	1	0	0	0	W	x	x	x	x	DDL				
R5	1	0	1	0	W	x	x	x	OEA		HDL			
R6	1	1	0	0	W	x	x	x	x	x	x	VCSL		
R7	1	1	1	0	W	x	x	x	x	GAM SEL	Reserved	VLNC	AVGY	Reserved
T0	0	0	0	1	W	x	AVDDADJ			PDTY		FBV2	FBV1	FBV0
T1	0	0	1	1	W	x	x	AVG	AVDDEN	T352	CONST			
T2	0	1	0	1	W	x	x	VDCEN	VCOMDC					
T3	0	1	1	1	W	x	x	BRADJ						
T4	1	0	0	1	W	x	x	x	x	x	x	Reserved	VNSEL	
T5	1	0	1	1	W	x	SAT				HUE			
T6	1	1	0	1	R	x	Reserved							

Note 1: Please keep all the Reserved registers at "**Default Value**" to avoid the abnormal display.

Note 2: Register T6 is read only.

c1 - Default register settings

No	D15	D14	D13	D12	D11	D[10 : 8]	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	x	x	x	x	x	1	1	0	1
R1	0	0	1	0	R/W	x	x	x	0	0	0	0	0	1
R2	0	1	0	0	R/W	x	x	x	x	x	0	0	1	1
R3	0	1	1	0	R/W	x	x	x	x	0	0	0	0	1
R4	1	0	0	0	R/W	x	x	x	x	0	0	0	0	0
R5	1	0	1	0	R/W	x	x	x	0	0	0	0	0	0
R6	1	1	0	0	R/W	x	x	x	x	x	x	1	1	0
R7	1	1	1	0	R/W	x	x	x	x	0	0	0	1	1
T0	0	0	0	1	R/W	x	0	0	0	0	0	1	0	0
T1	0	0	1	1	R/W	x	x	0	0	0	1	0	0	0
T2	0	1	0	1	R/W	x	x	0	1	0	0	0	0	0
T3	0	1	1	1	R/W	x	x	1	0	0	0	0	0	0
T4	1	0	0	1	R/W	x	x	x	x	x	x	0	0	0
T5	1	0	1	1	R/W	x	1	0	0	0	1	0	0	0
T6	1	1	0	1	R	x	Reserved							

"X" => Don't care.

d. Detail Register Description

d1. Register R0

Address	Bit	Description		Default
0000	[3..0]	Bit3 (GRB)	Global reset	1101b
		Bit2 (STB)	Stand-by mode setting	
		Bit1 (SHDB)	DC-DC converter shutdown setting	
		Bit0 (SHCB)	Charge Pump shutdown setting	

Bit3	GRB function
0	Controller is reset, and the charge pump and DCDC is off. Reset all registers to default values.
1	Normal operation (default)

Bit2	STB function
0	T-CON, source driver and DC-DC converter are off. All outputs are High-Z.
1	Normal operation (default)

Bit1	SHDB function
0	DC-DC converter is off. (default)
1	DC-DC converter is on. DC-DC controls by STB and power on/off sequence.

Bit0	SHCB function
0	Charge Pump converter is off.
1	Charge Pump converter is on. (default) Charge Pump controls by STB and power on/off sequence.

d2. Register R1:

Address	Bit	Description		Default
0010	[5..0]	Reserved	Reserved	00_0001b
		Reserved	Reserved	
		Bit1 (PFON)	Pre-filter setting	
		Reserved	Reserved	

Bit1	Pre-filter setting.
0	Pre-filter off (default)
1	Pre-filter on

d3. Register R2:

Address	Bit	Description		Default
0100	[3..0]	Bit3 (FPOL)	FRP source driver polarity inversion polarity inversion selection.	0011b
		Reserved	Reserved	
		Bit1 (U/D)	Vertical shift direction selection.	
		Bit0 (SHL)	Horizontal shift direction selection.	

Bit3	FPOL function
0	FRP = 0 in positive polarity FRP = 1 in negative polarity (default)
1	FRP = 1 in positive polarity FRP = 0 in negative polarity

Bit1	UD function
0	Scan down: First line = G241 → G239 → … → G2 → Last line = G0.
1	Scan up: First line=G0→ G2 →…→ G239 → Last line=G241. (default)

Bit0	SHL function
0	Shift left; First data = S640 → S639 → …→ S2 → Last data = S1.
1	Shift right: First data = S1→ S2 → …→ S639→ Last data = S640 (default)

d4. Register R3:

Address	Bit	Description		Default
0110	[4..0]	Bit4 (PALM)	PAL 1/6, PAL1/6, 8 select	1_0001b
		Bit3 (PAL)	PAL/NTSC selection.	
		Bit2-0 (SEL)	Input data format selection.	

Bit4	PALM function
0	PAL 1/6, Input format (280 active line).
1	PAL1/6 Input format (288 active line), (default)

Bit3	PAL function
0	NTSC Input format (240 active line), (default)
1	PAL Input format

Bit2-0	SEL function
000	UPS051 path, special data format: DDX
001	UPS052 320RGB 24.54MHz data format (default)
010	UPS052 360RGB 27MHz data format
011	YUV mode A 640Y 320CrCb 24.54MHz data format
100	YUV mode A 720Y 360CrCb 27MHz data format
101	YUV mode B 640Y 320CrCb 24.54MHz data format
110	YUV mode B 720Y 360CrCb 27MHz data format
111	CCIR 656 720Y 360CrCb 27MHz data format

d5. Register R4:

Address	Bit	Description		Default
1000	[4..0]	Bit4-0 (DDL)	Horizontal Data start delay selection	0_0000b

D4	D3	D2	D1	D0	Value	Unit
0	0	0	0	0	+0 (default)	DCLK
0	0	0	0	1	**+1**	
0	0	0	1	0	+2	
0	0	0	1	1	+3	
0	0	1	0	0	+4	
0	0	1	0	1	+5	
0	0	1	1	0	+6	
0	0	1	1	1	+7	
0	1	0	0	0	+8	
0	1	0	0	1	+9	
0	1	0	1	0	+10	
0	1	0	1	1	+11	
0	1	1	0	0	+12	
0	1	1	0	1	+13	
0	1	1	1	0	+14	
0	1	1	1	1	+15	
1	0	0	0	0	-1	
1	0	0	0	1	-2	
1	0	0	1	0	-3	
1	0	0	1	1	-4	
1	0	1	0	0	-5	
1	0	1	0	1	-6	
1	0	1	1	0	-7	
1	0	1	1	1	-8	
1	1	0	0	0	-9	
1	1	0	0	1	-10	

1	1	0	1	0	-11	
1	1	0	1	1	-12	
1	1	1	0	0	-13	
1	1	1	0	1	-14	
1	1	1	1	0	-15	
1	1	1	1	1	-16	

d6. Register R5:

Address	Bit	Description		Default
1010	[5..0]	Bit5-4 (OEA)	Odd Even advance selection	00_0000b
		Bit3-0 (HDL)	Vertical delay selection	

Bit5-4	OEA function
00	Display start @ HDL delay for Odd and Even field (default)
01	Display start @ HDL delay for Odd field and @ HDL+1 for Even field
1X	Display start @ HDL+1 delay for Odd field and @ HDL+1 for Even field

Bit3-0	HDL function				
HDL3	HDL2	HDL1	HDL0	Value	Unit
0	0	0	0	+0 (default)	H
0	0	0	1	+1	
0	0	1	0	+2	
0	0	1	1	+3	
0	1	0	0	+4	
0	1	0	1	+5	
0	1	1	0	+6	
0	1	1	1	+7	
1	0	0	0	+8	
1	0	0	1	-1	
1	0	1	0	-2	
1	0	1	1	-3	
1	1	0	0	-4	
1	1	0	1	-5	
1	1	1	0	-6	
1	1	1	1	-7	

d7. Register R6:

Address	Bit	Description		Default
1100	[2..0]	Bit2-0 (VCOM_AC)	VCAC level adjustment. Step 0.2V/LSB.	110b

VCSL2	VCSL1	VCSL0	VCAC level	Unit
0	0	0	6.2	V
0	0	1	6.4	
0	1	0	5.0	
0	1	1	5.2	
1	0	0	5.4	
1	0	1	5.6	
1	1	0	5.8 (default)	
1	1	1	6.0	

d8. Register R7:

Address	Bit	Description		Default
1110	[4..0]	Bit4 (GAMSEL)	Gamma select function	0_0011
		Reserved	Reserved	
		Bit2 (VLNC)	YUV vertical line function	
		Bit1 (AVGY)	Average YUV interface Luminance Y setting	
		Bit0 (DMDA)	Delta data alignment	

Bit4	Gamma select function
0	Non- Linear Gamma (default)
1	Gamma 2.2

Bit2	YUV vertical line function
0	Vertical line are 240 (default)
1	Vertical line are 234 NTSC: 240 lines scaling to 234-skip 6 lines (1/40) PAL: 288 lines scaling to 234-skip 54 lines (3/16) @ PALM = 'H' 280 lines scaling to 234-skip 46 lines (1/6) @ PALM = 'L'

Bit1	Average YUV interface Luminance Y setting
0	Only use odd Y sample for YUV conversion
1	Use odd and even Y sample for YUC conversion (default)

Bit0	Delta data alignment
0	Data alignment by default setting
1	Data alignment please reference UPS052 timing graph II (default). (This function disable in UPS051 mode.)

d9. Register T0:

Address	Bit	Description		Default
0001	[7..0]	Bit5-7 (AVDDADJ)	Select internal AVDD voltage	0000_0100b
		Bit3-4 (PDTY)	PWM duty control for DC to DC converter	
		Bit2-0 (FBV)	FB voltage adjust	

Bit 5- 7	Select internal AVDD voltage
000	3.3V (default)
001	3.5V
010	3.7V
011	3.9V
100	4.1V
101	4.3V
110	4.5V
111	4.7V

Bit3-4	PWM duty control for DC to DC converter
00	75 %(Default)
01	55 %
10	60 %
11	65 %

Bit2-0	FB voltage adjust
000	0.4V
001	0.45V
010	0.5V
011	0.55V
100	0.6V (default)
101	0.65V
110	0.7V
111	0.75V

d10. Register T1:

Address	Bit	Description		Default
0011	[6..0]	Bit6 (AVG)	Data alignment to scaling down function select	000_1000b
		Bit5 (AVDDEN)	Enable internal AVDD	
		Bit4 (T352)	Select UPS052 path and input data format for 352 RGB	
		Bit3-0 (CONST)	RGB contrast level adjustment	

Bit6	Data alignment to scaling down function select
0	Data alignment by DMDA settling (Default)
1	Data alignment with averaged and input data. (R1, (G1+3G2)/4, (3B2+B3)/4…….)

Bit5	Enable internal AVDD
0	Select external AVDD(Default)
1	Select internal AVDD

Bit4	Select UPS052 path and input data format for 352 RGB
0	SEL setting timing (Default)
1	SEL setting don't care, input data for 352 RGB (27MHZ)

Bit3-0	RGB contrast level adjustment
0x0	0
0x8	1.00 (default)
0xF	1.875

d11. Register T2:

Address	Bit	Description		Default
0101	[6..0]	Bit6 (VDCEN)	Setting FRP output to add DC level	010_0000b
		Bit5-0 (VCOM DC)	VCOM DC level adjustment (16mV/Bit)	

Bit6	Setting FRP output to add DC level
0	External VCOM DC (Default)
1	Internal VCOM DC

Bit5-0	VCOM DC level adjustment
0x00	0.188V
0x20	0.7V (Default)
0x3F	1.196V

d12. Register T3:

Address	Bit	Description		Default
0111	[6..0]	Bit6-0 (BRADJ)	Brightness level adjustment (4/Bit)	100_0000b

Bit6	Brightness level adjustment
0x00	-256
0x40	0 (default)
0x7F	+256

d13. Register T4:

Address	Bit	Description		Default
1001	[2..0]	Reserved	Reserved	000b
		Bit1-0 (WNSEL)	Wide and narrow display select	

Bit1-0	Wide and narrow display select
00	Normal display (default)
01	Narrow display
10	Wide display
11	Normal display

d14. Register T5:

Address	Bit	Description		Default
1011	[7..0]	Bit7-4 (SAT)	YUV saturation constant adjustment (0.125/Bit)	1000_1000b
		Bit3-0 (HUE)	YUV Hue adjustment (5Deg/Bit)	

Bit7-4	YUV saturation constant adjustment
0x0	0
0x8	1.00 (default)
0xF	1.875

Bit3-0	YUV Hue adjustment (5Deg/Bit)
0x0	-40θ°
0x8	0θ° (default)
0xF	35 θ°

Note: Register T5 is for YUV only.

C. Optical specification (Note 1, Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise Fall	 Tr Tf	 θ=0°	 - -	 25 30	 50 60	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	120	300	-		Note 5,6
Viewing angle Top Bottom Left Right		CR≧10	 10 30 40 40	 15 35 45 45	 - - - -	deg.	Note 7
Brightness (25mV)	Y_L	θ=0°	200	250	-	cd/m^2	Note 8
White chromaticity	x	θ=0°	(0.26)	(0.31)	(0.36)		
	y	θ=0°	(0.28)	(0.33)	(0.38)		

Note 1. Ambient temperature = 25℃.

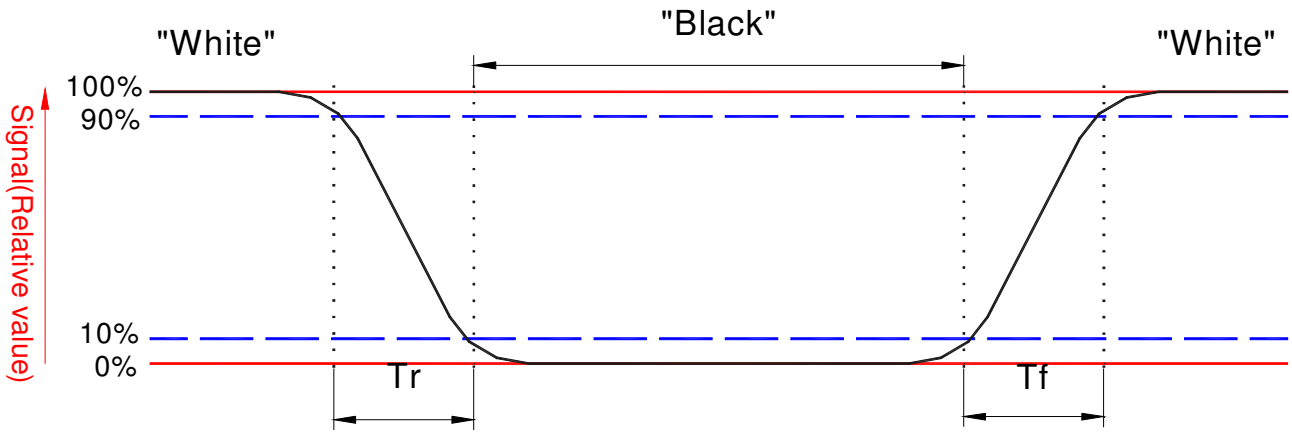
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of the panel with a field angle of 1° by Topcon luminance meter M-7, after 10 minutes operation.

Note 4. Definition of response time:

Output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black” (rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refere to figure as follows:



Note 5. Definition of contrast ratio:

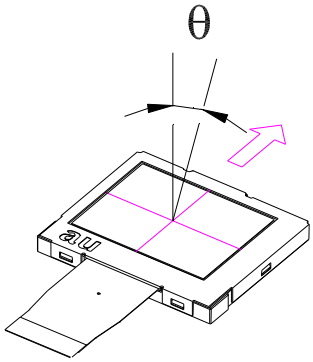
Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White Vi = V_{i50} ∓ 1.5V
Black Vi = V_{i50} ± 2.0V
"±" means that the analog input signal swings in phase with COM signal.

" ∓ means that the analog input signal swings out of phase with COM signal.
V_{i50} : The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:
Refer to figure as below.



Note 8. Measure at the center area of the panel when all the input terminals of LCD panel are electrically opened.

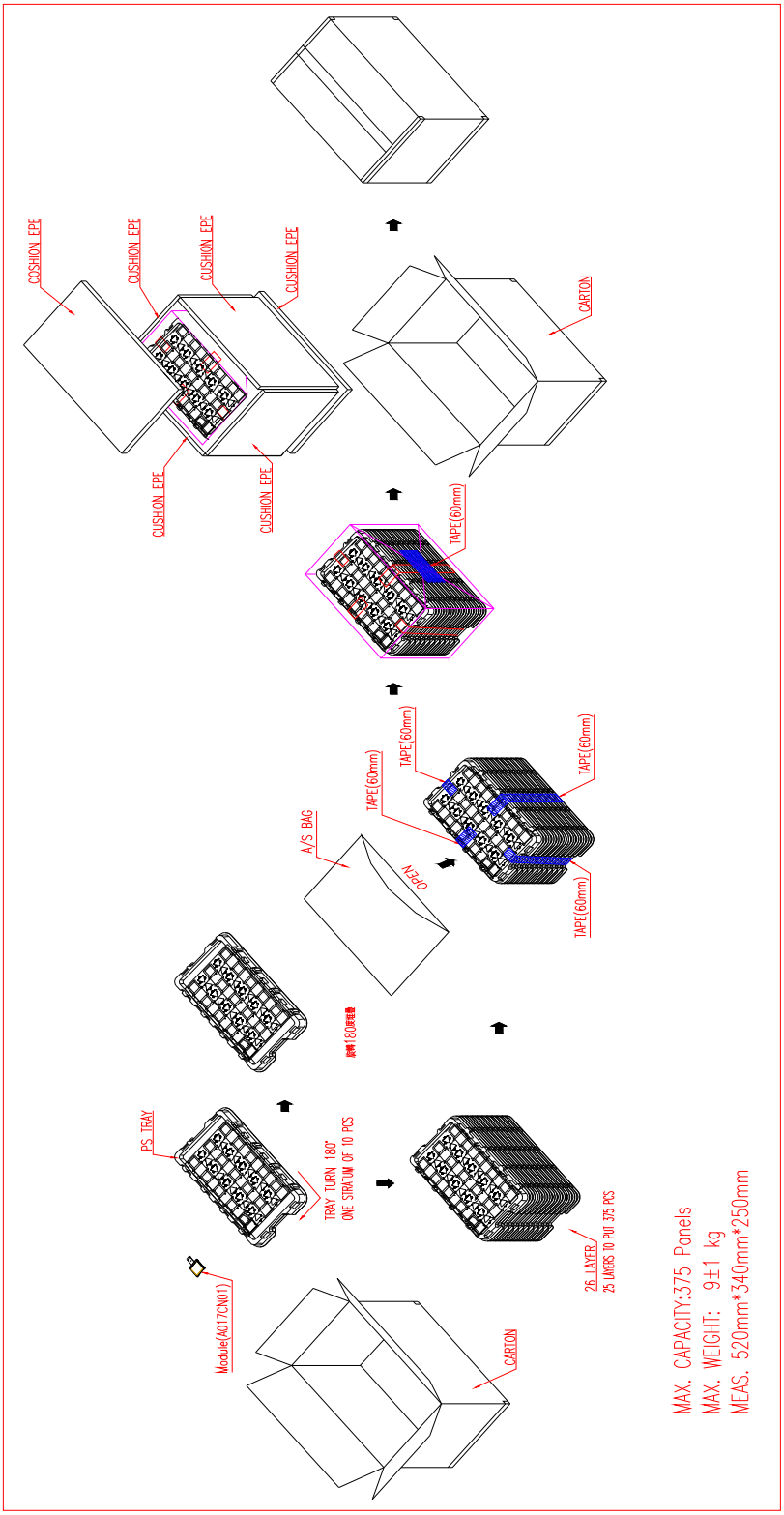
D. Reliability test items

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

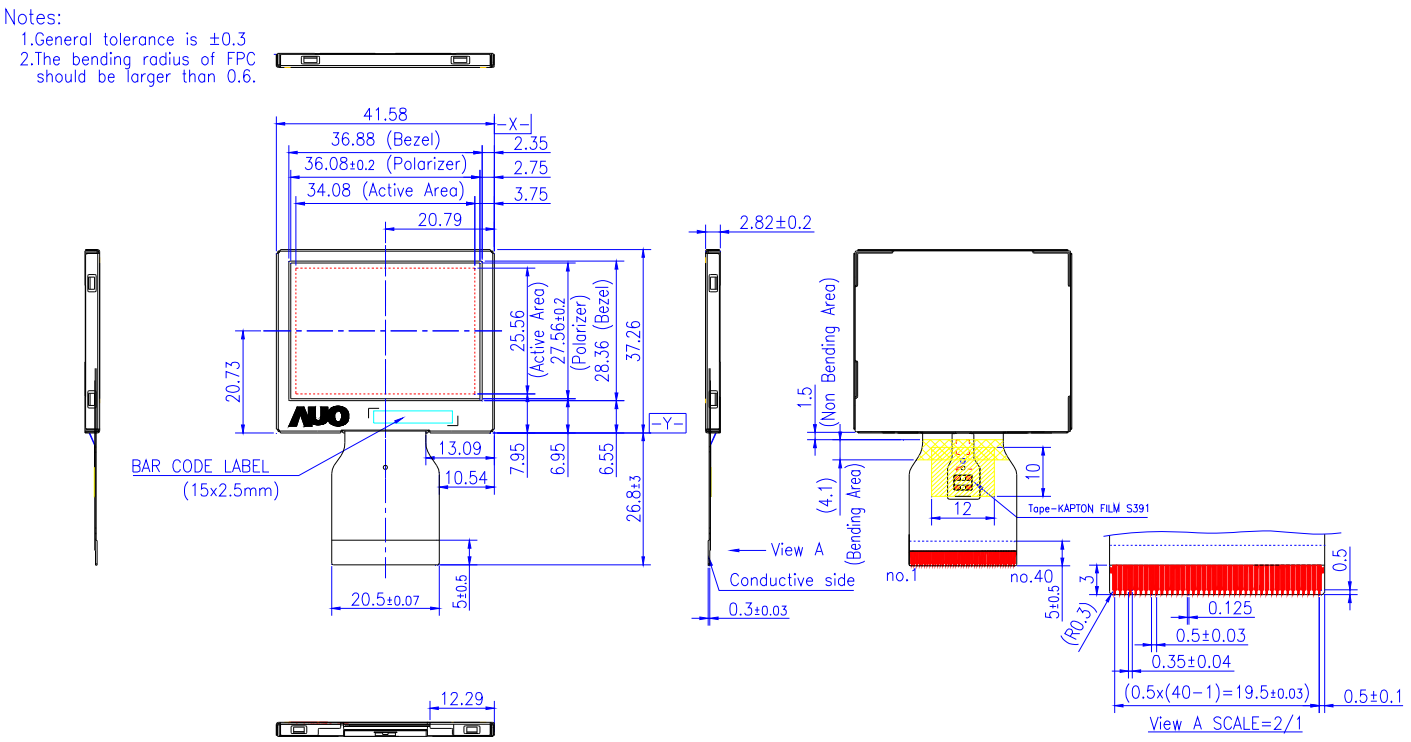
Note 1： Ta：Ambient temperature.

Note 2： It is forbidden to squeeze the panel when designing mechanical structure related to panel itself.

E. Packing form



F. Outline dimension



"To avoid applying pressure or stress on the products. These will cause visual defects or luminance non-uniformity on the lighting area."

G. Application Notes

1. Stand-by timing

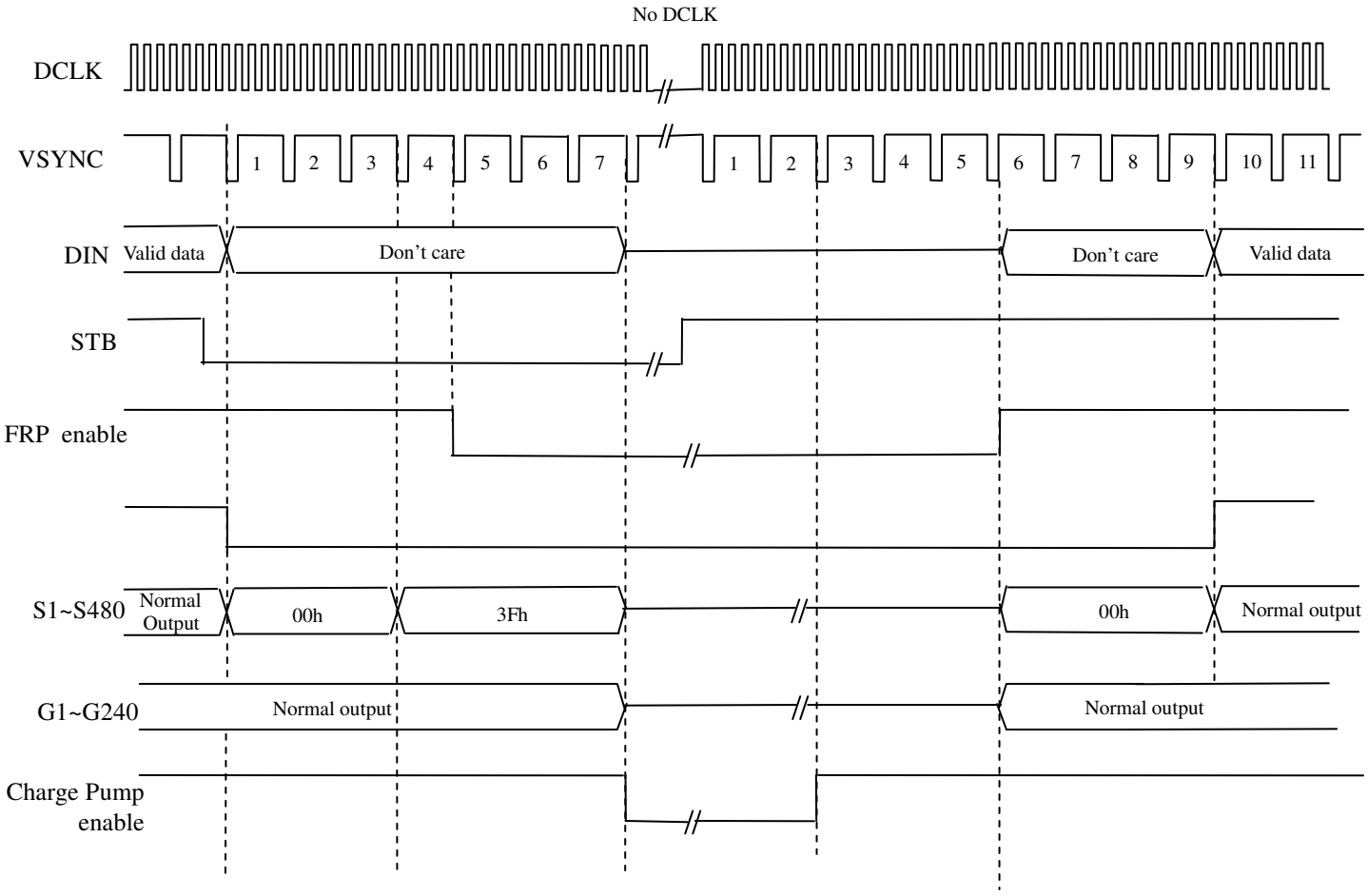


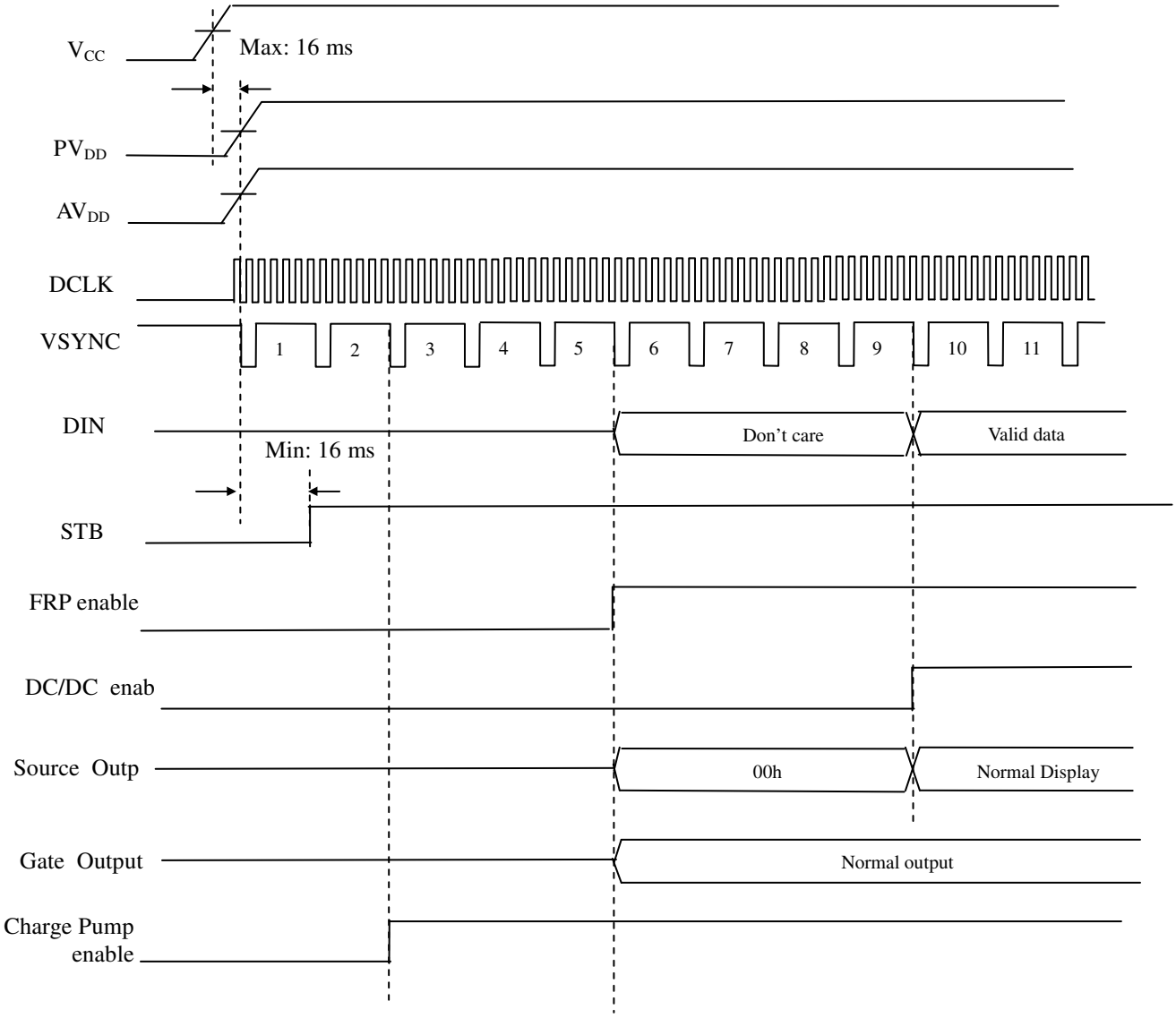
Figure 1: Stand-by timing diagram

Note 1: During no DCLK, HSYNC and VSYNC can be stopped. But in all other cases HSYNC and VSYNC must be active.

Note 2: External signal: DCLK, VSYNC, DIN (D0 ~ D7), STB (By register)

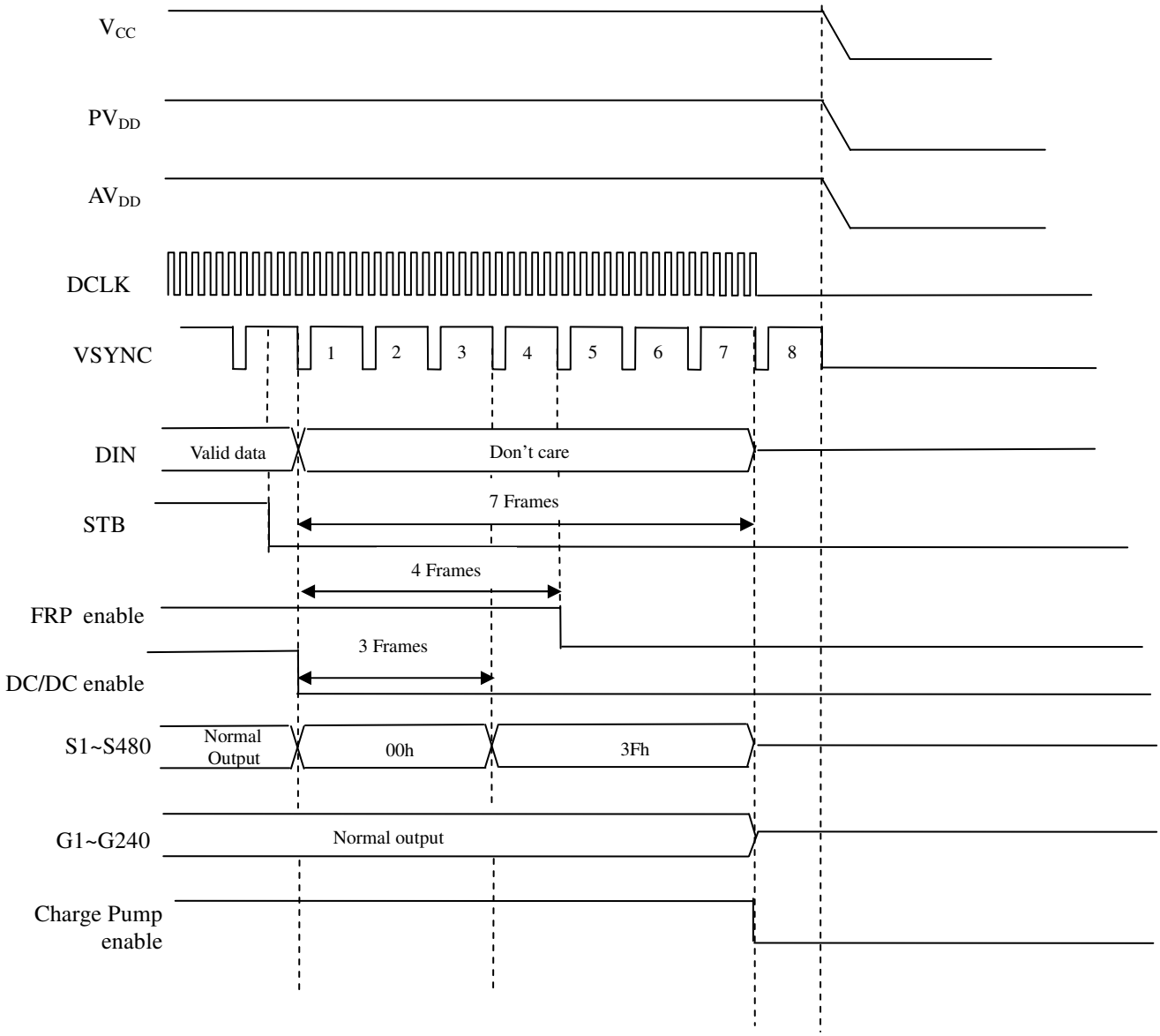
Internal signal: DC/DC enable S1 ~ S480 (Source Driver output signal), FRP enable G1 ~ G240 (Gate Driver output signal) and Charge Pump enable

2. Power on sequence



Note 1: External signal: $V_{CC,}$ $PV_{DD,}$ AV_{DD}, DCLK, VSYNC, DIN (D0 ~ D7), STB (By register)
Internal signal: DC/DC enable S1 ~ S480 (Source Driver output signal), FRP enable,
G1 ~ G240 (Gate Driver output signal) and Charge Pump enable.

3. Power off sequence

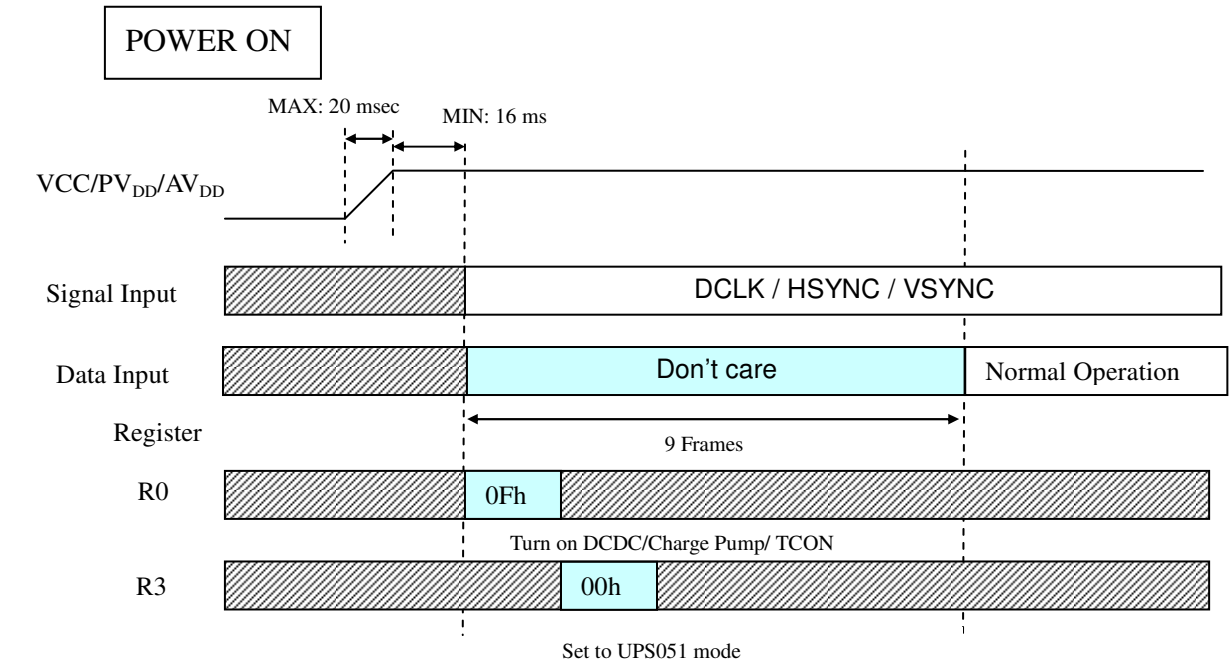


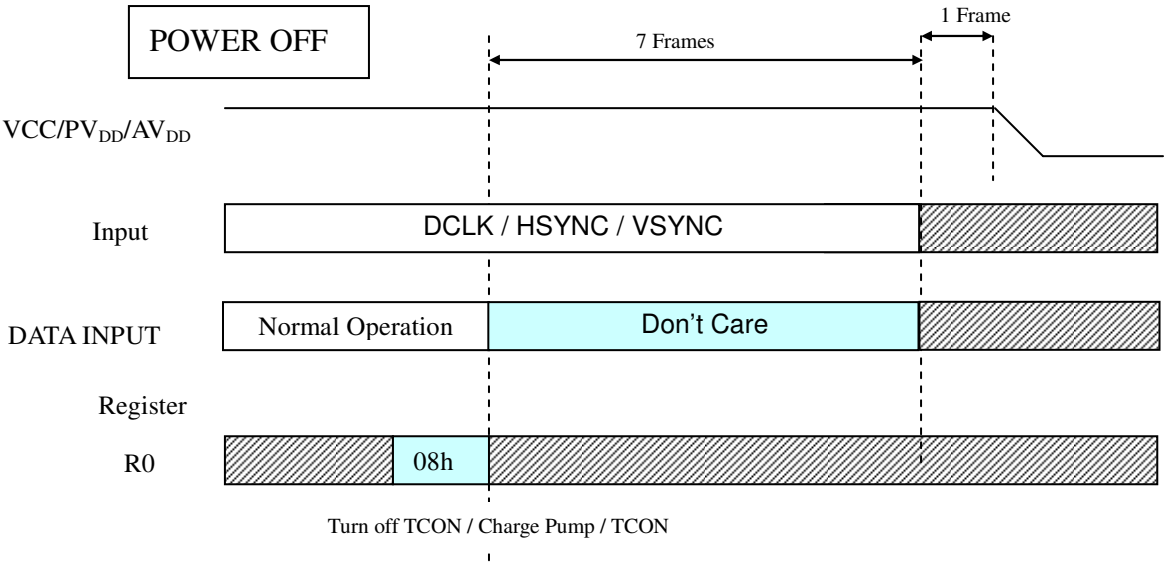
Note 1: External signal: $V_{CC,}$ $PV_{DD,}$ AV_{DD}, DCLK, VSYNC, DIN (D0 ~ D7), STB (By register)

Internal signal: DC/DC enable S1 ~ S480 (Source Driver output signal), FRP enable,

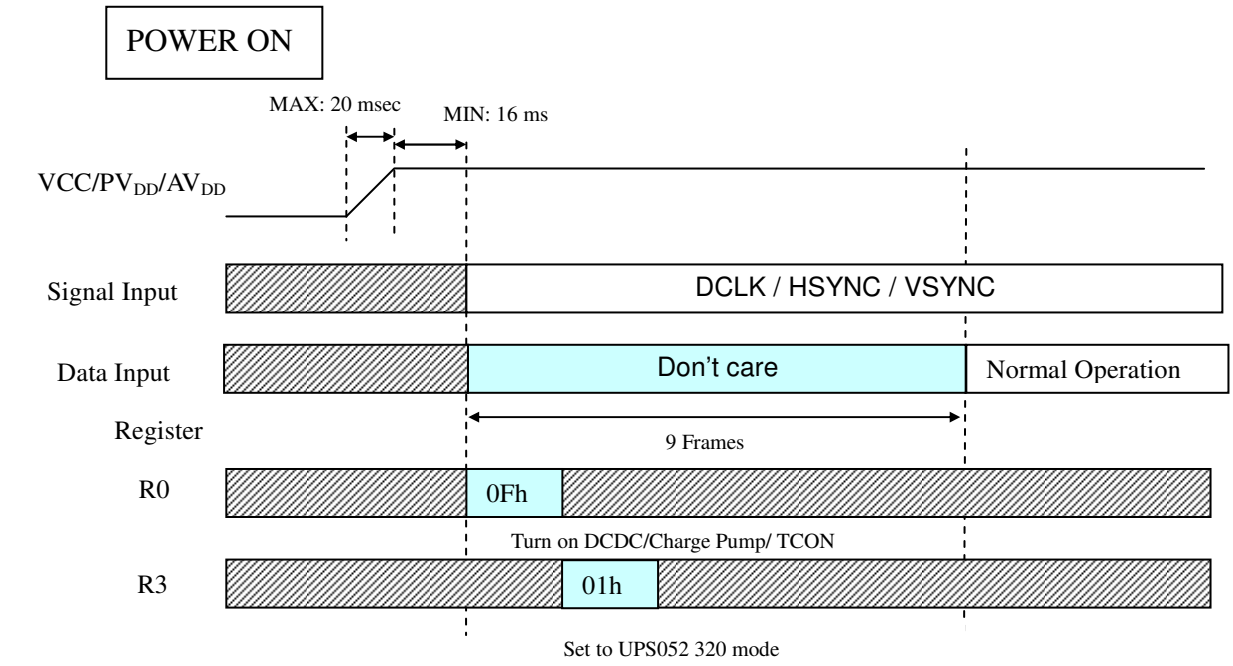
G1 ~ G240 (Gate Driver output signal) and Charge Pump enable.

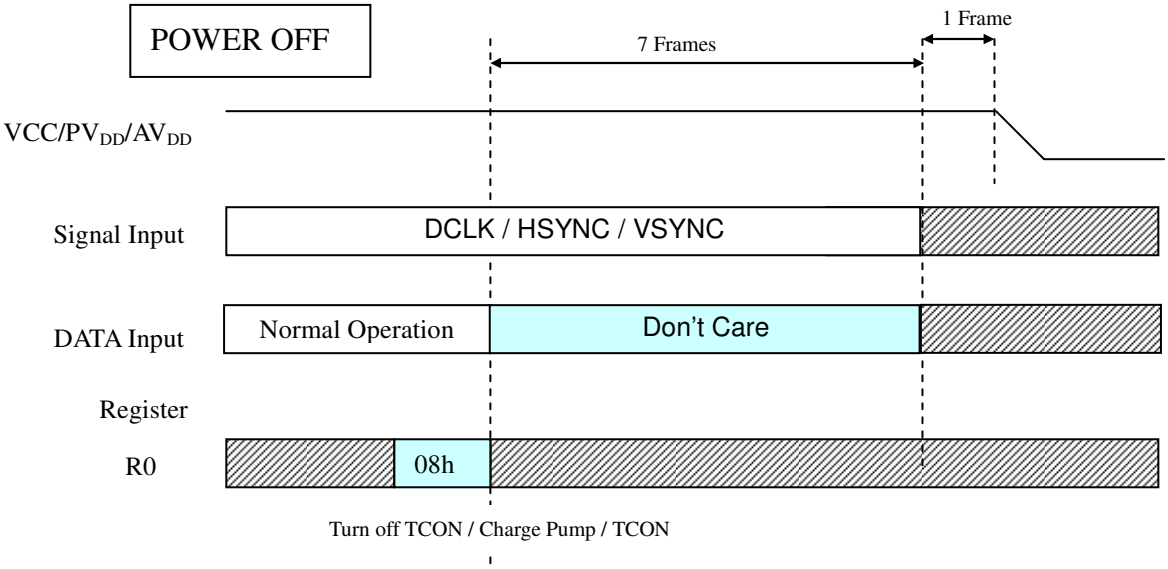
3. Recommend UPS051 (9.7 MHz) power on/off setting



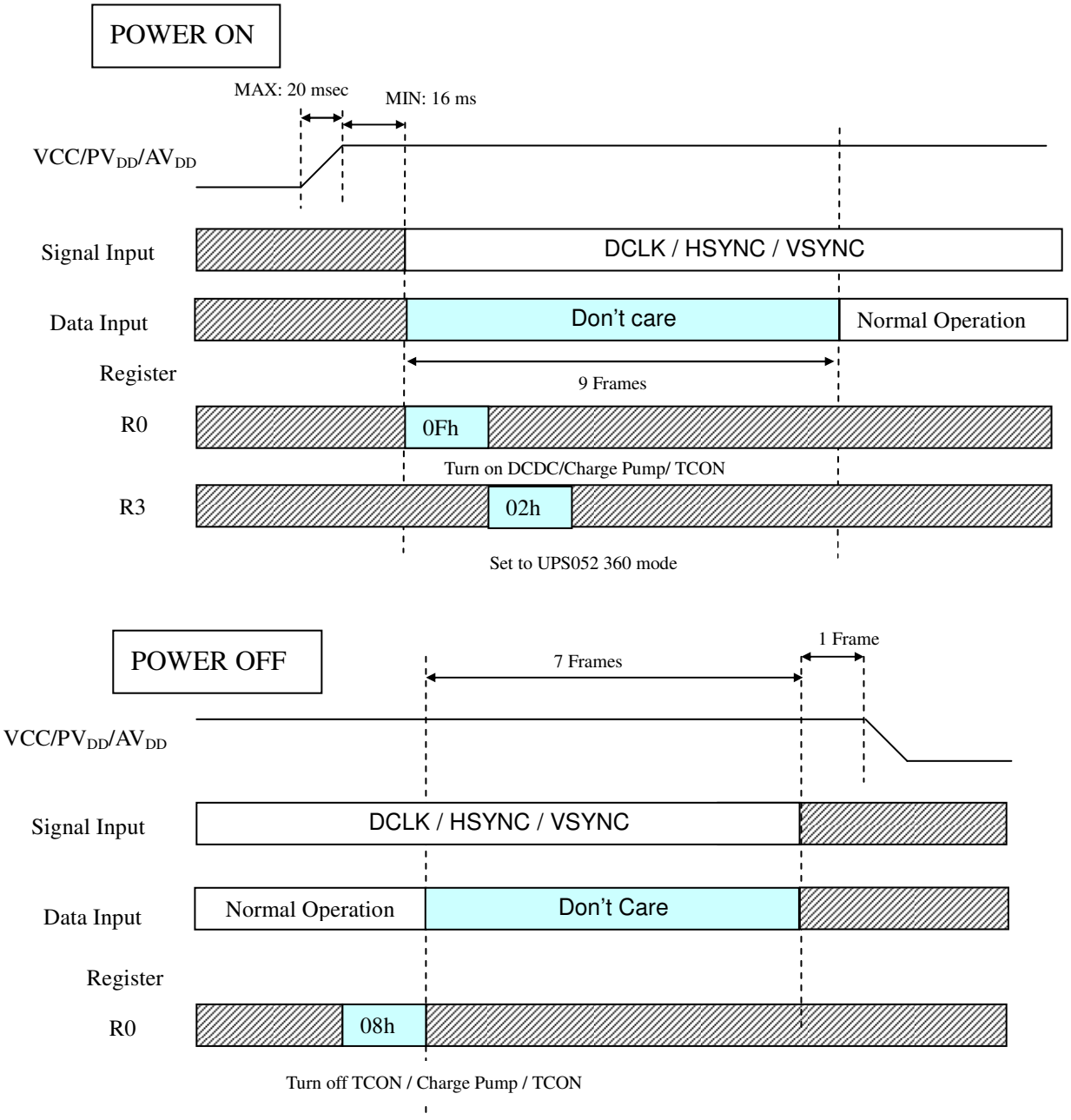


4. Recommend UPS052 320RGB mode (24.54 MHz) power on/off setting

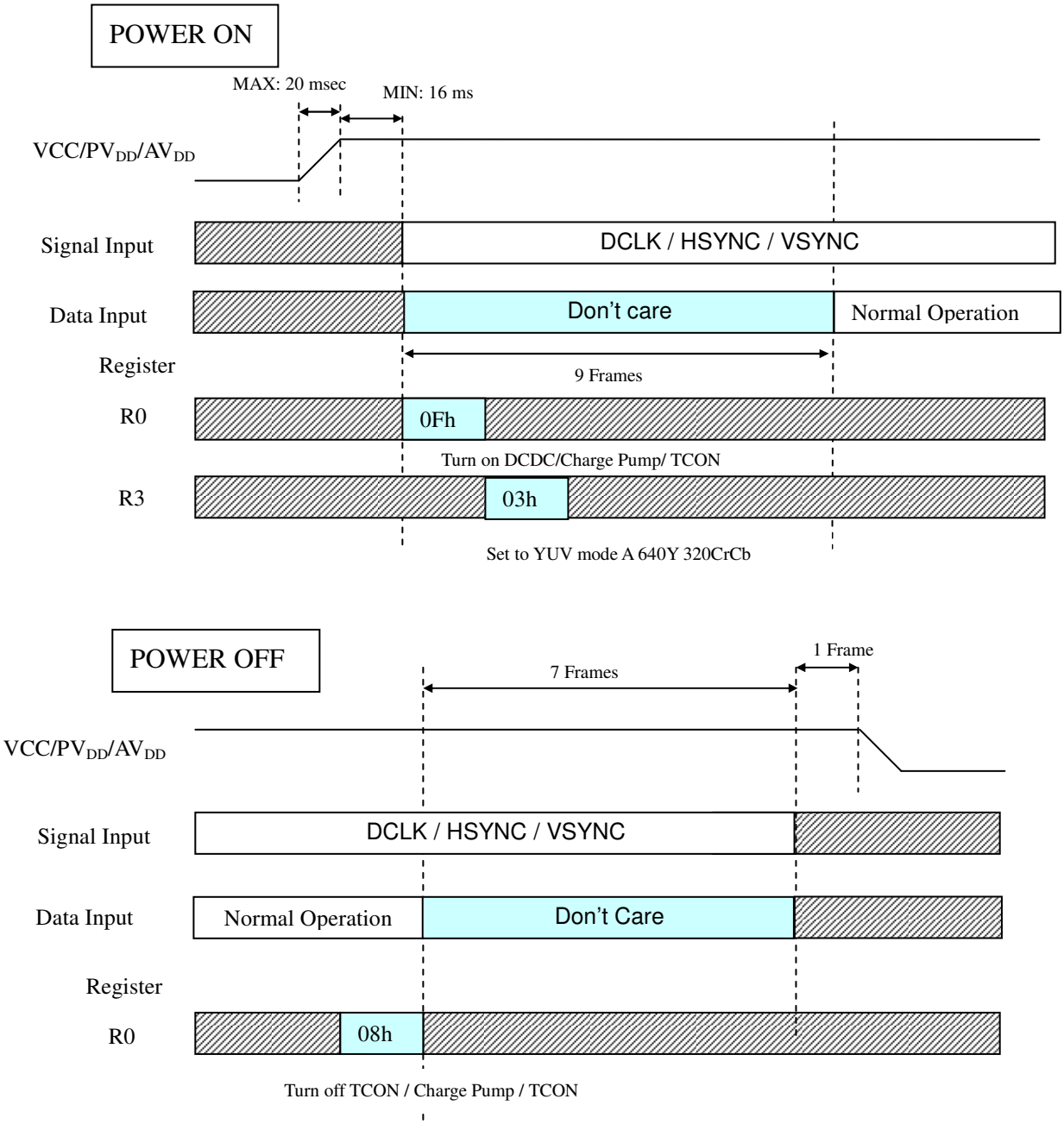




5. Recommend UPS052 360RGB mode (27MHz) power on/off setting

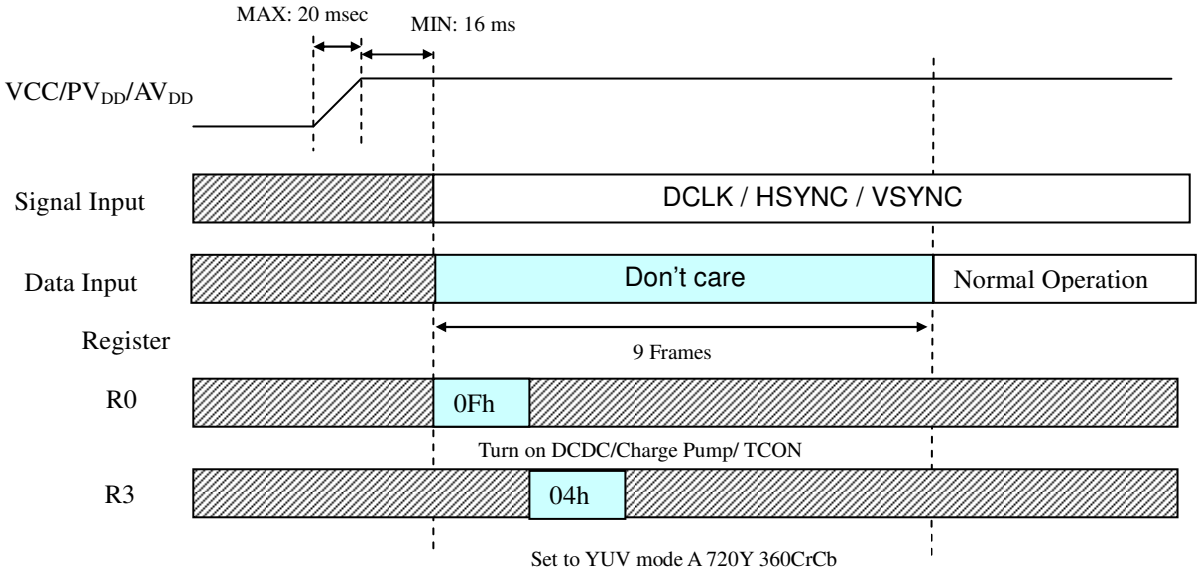


6. Recommend YUV mode A 640Y 320CrCb (24.54 MHz) power on/off setting

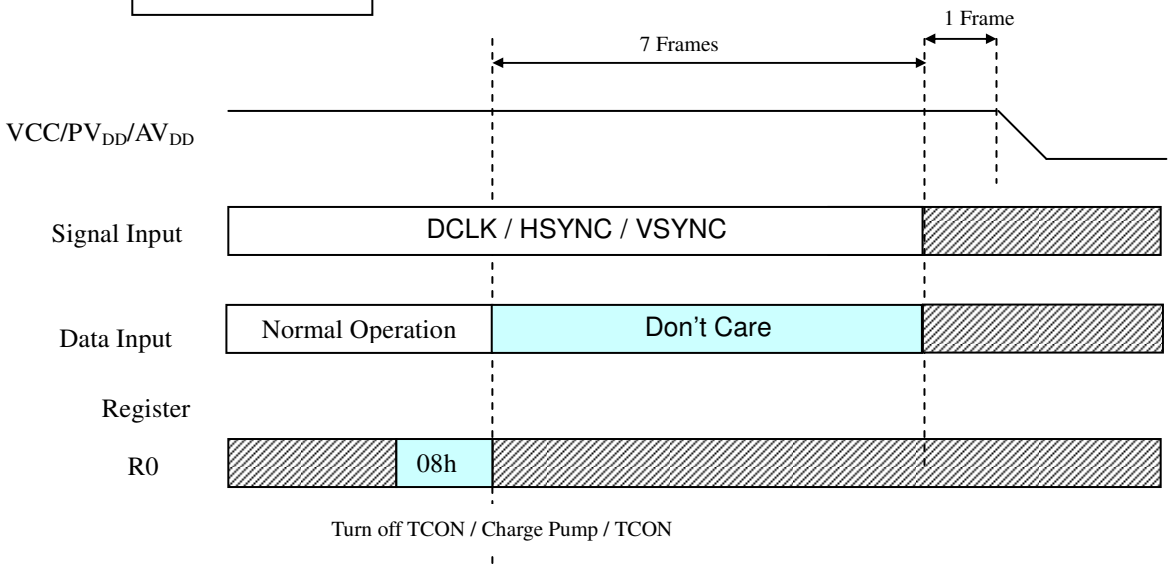


7. Recommend YUV mode A 720Y 360CrCb (27 MHz) power on/off setting

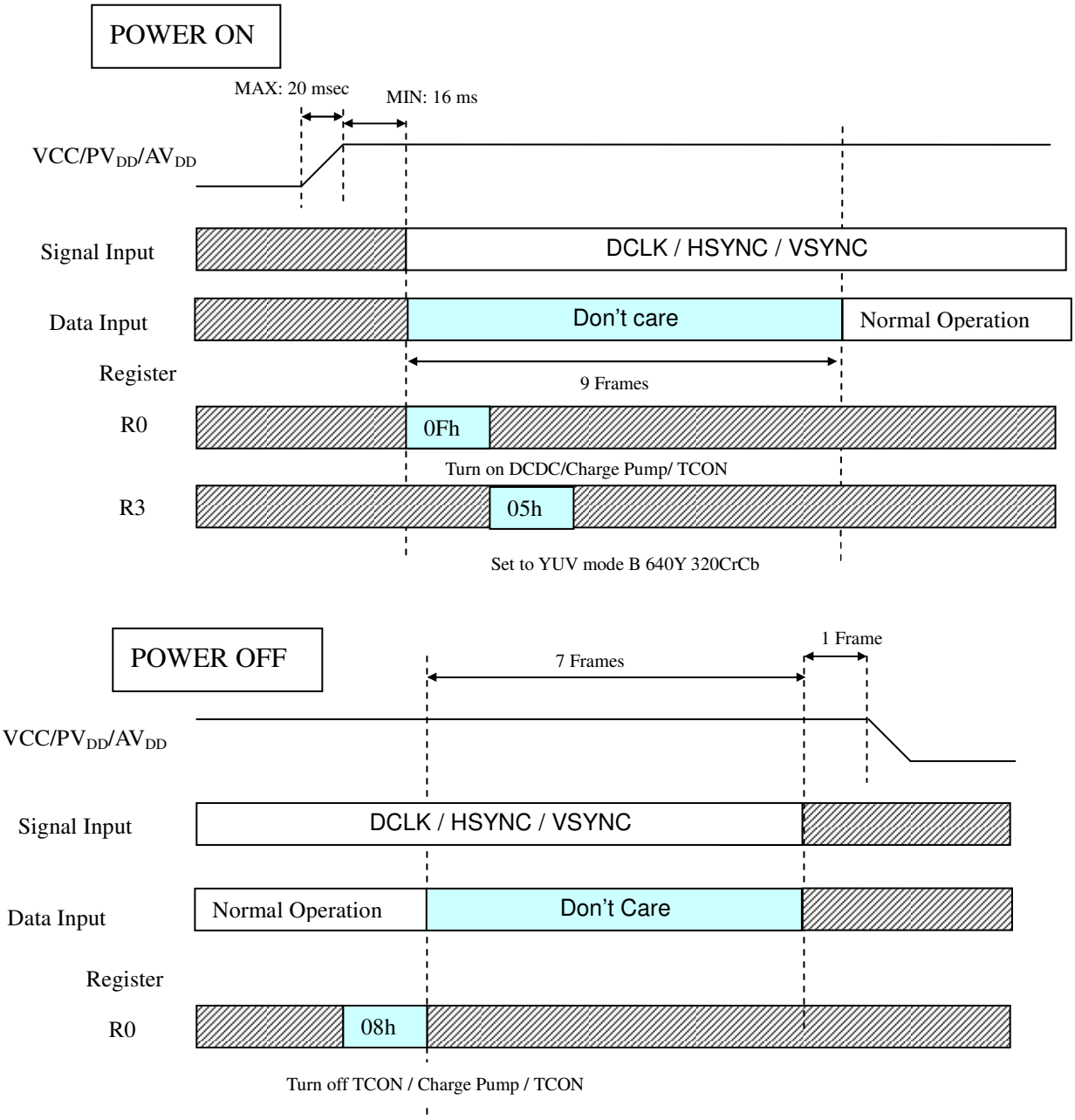
POWER ON



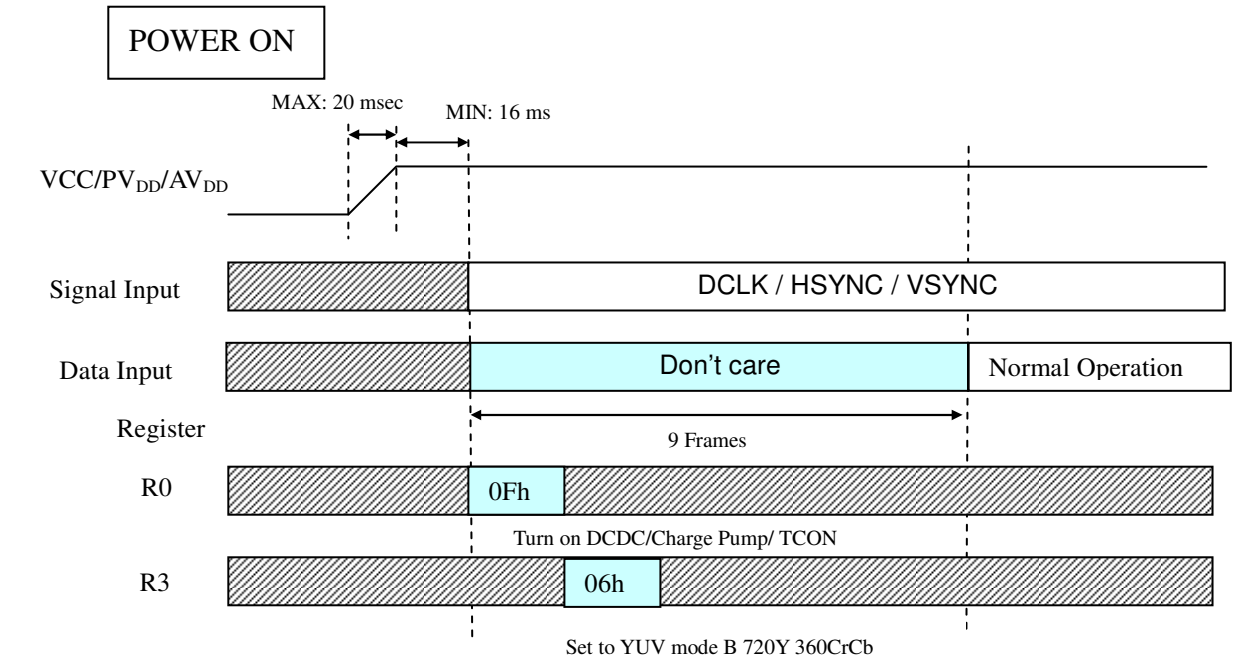
POWER OFF

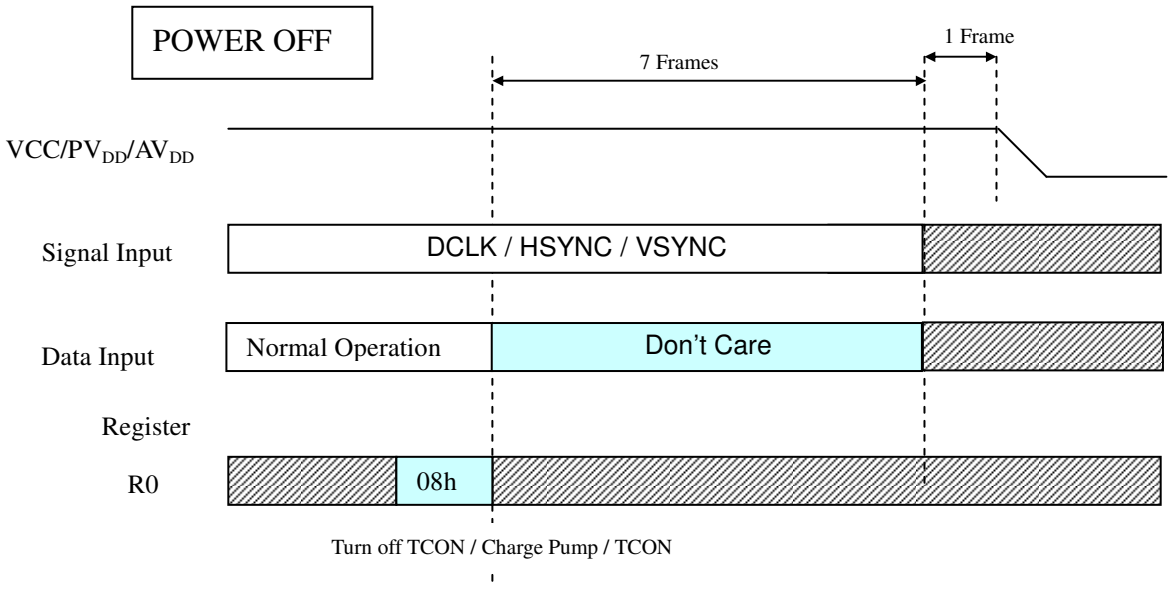


8. Recommend YUV mode B 640Y 320CrCb (24.54 MHz) power on/off setting



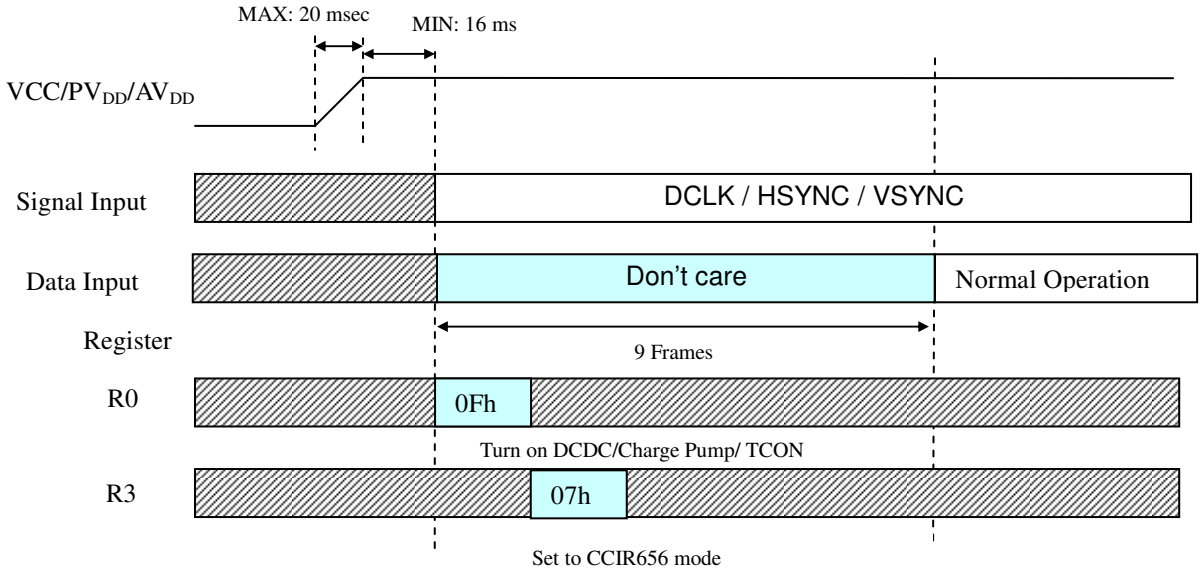
9. Recommend YUV mode B 720Y 320CrCb (27 MHz) power on/off setting



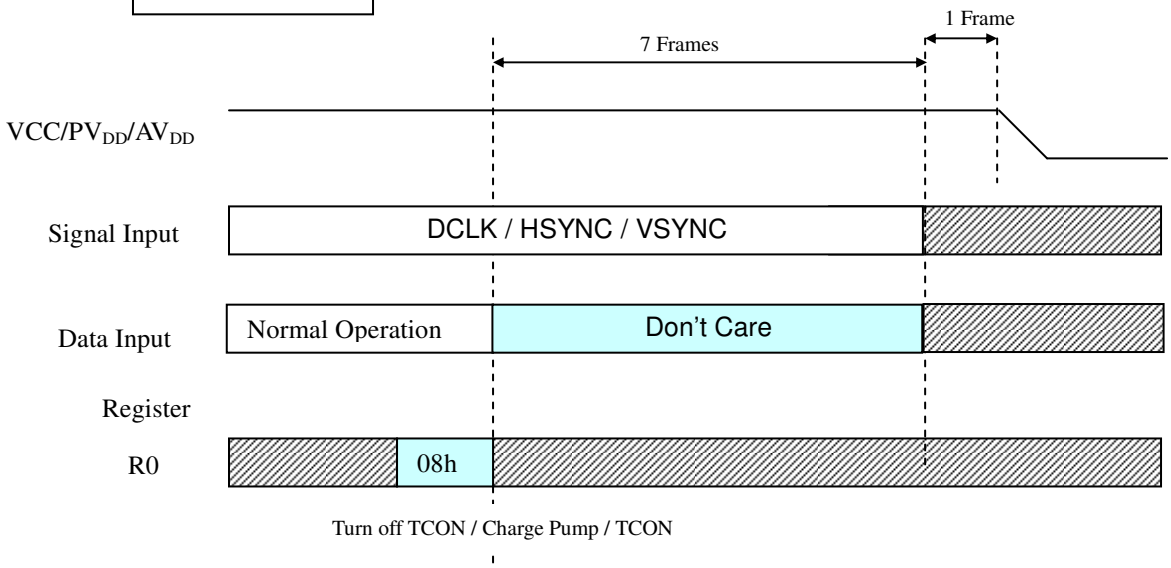


10. Recommend CCIR656 mode (27 MHz) power on/off setting

POWER ON



POWER OFF

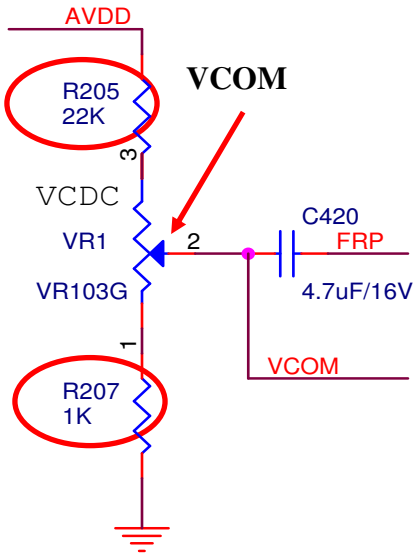


11. Difference between This model and Previous models (A017CN01 V0 ~ V2)

a. VCOM DC setting

Because the structure of ASIC is different between the new model and original one,

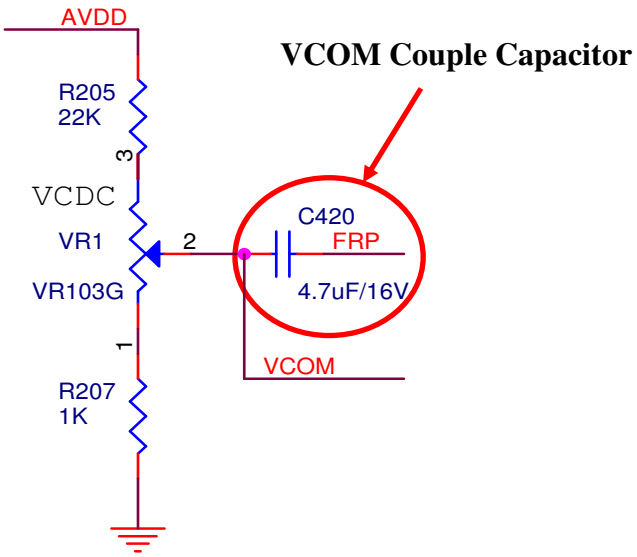
AUO suggests customers adjusting VCOM DC value from 0.45V±0.2 to 0.8V±0.2 to get the best display quality.



b. VCOM Couple capacitor

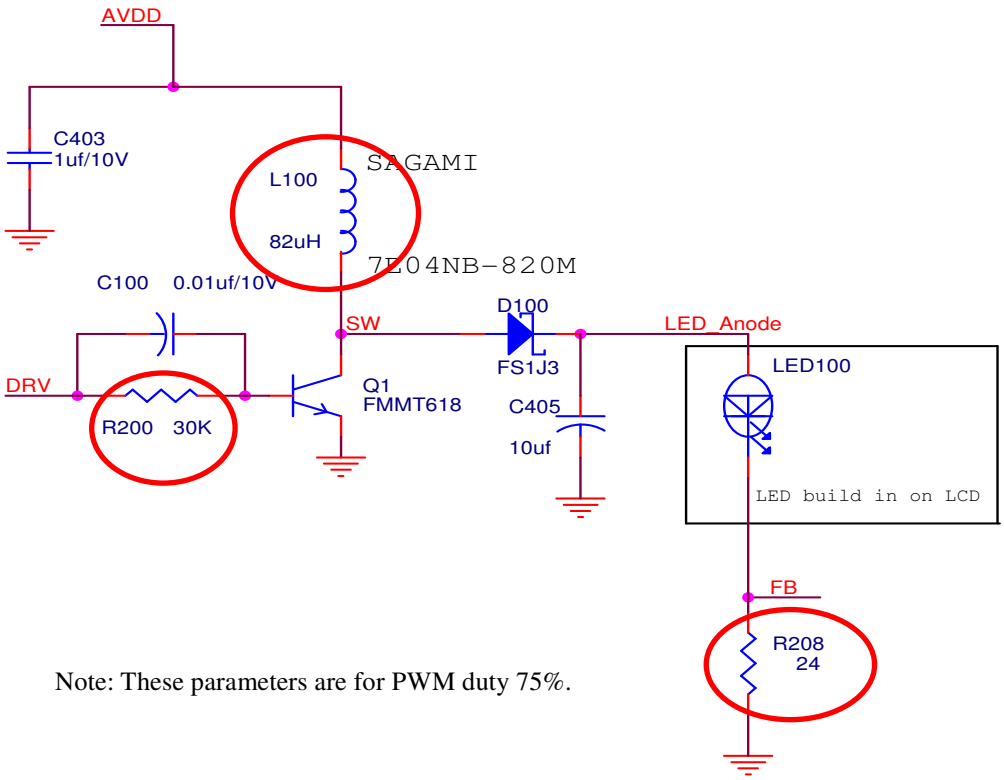
Original panel structure is Cst on gate and the new model is Cst on common.

To avoid Horizontal Cross Talk, AUO suggests modifying VCOM couple capacitor (C420) from 1uF to 4.7uF.



c. PWM RC Parameters

AUO suggests fine-tuning PWM RC parameters to get the best display performance. By the way, please modify R208 from 30 ohm to 24 ohm to get 25 mA LED current. About the recommend RC Parameters, please refer to the following figure.



Note: These parameters are for PWM duty 75%.

d. ESD Protection

a. AUO suggests always sending serial commend to avoid shutdown phenomenon.

b. AUO suggests connecting iron shell to system GND to enhance ESD protection ability.